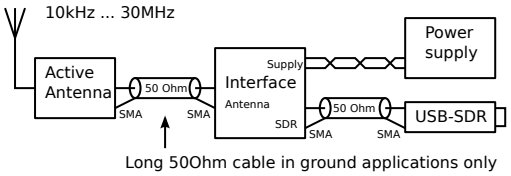
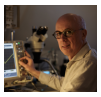
Design of a LF-HF Active Antenna in CMOS18 technology

Radio astronomy antenna for space applications



Antenna length: max 0.5m
E-field antenna-referred noise:
10kHz : 100n
100KHz : 10n
1MHz : 5n
30MHz : 5n
$\left[\frac{\mathrm{V}}{\mathrm{m}\sqrt{\mathrm{Hz}}}\right]$
Output 1dB compression level:
0dBm in 50Ohm
Antenna gain (-3dB: 10kHz-30MHz)
0dB



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Features
ESD discharge protected
Low-power 1.8V CMOS technology

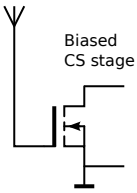
Structured step-by-step design

Step 1: can this active antenna be realized in a CMOS18 process?

1a. Can we meet the noise requirements in CMOS18 technology?
- if no: show stopper!
- if yes: find range for W, L and operating current of a transistor (NMOS18 and/or PMOS18)

Interpretation of the requirements:

$$S_{en} \approx 25 \cdot 10^{-18}\left(1+\left(\frac{200\cdot 10^3}{f}\right)^2\right)$$



Answer: Noise requirements can be met!
A large number of combinations of W, L and ID apply
(see SLiCAP results)

Best possible noise performance if input capacitance of NMOS equals antenna (source) capacitance: $c_{iss} = C_A$

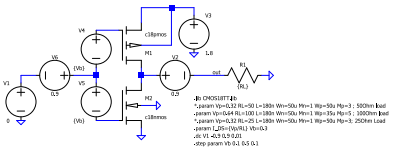
Feasible if: $\frac{8}{3}\mathrm{KF} < S_{en,f} L_A^2 f_\ell C_A$

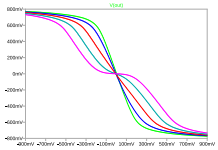
where:	$\mathrm{KF}[\mathrm{J}]$	Flicker noise coefficient CMOS18 process:
	$S_{en,f}\left[\frac{\mathrm{V}^2}{\mathrm{m}^2\mathrm{Hz}}\right]$	Spectral density of antenna-referred e-field floor noise
	$L_A[\mathrm{m}]$	Antenna length
	$f_\ell[\mathrm{Hz}]$	Floor noise low-frequency corner frequency
	$C_A[\mathrm{F}]$	Antenna capacitance

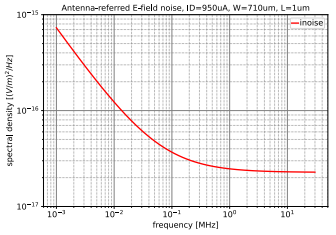
1b. Can we produce 0dBm output power in 50Ohm using 1.8V supply and CMOS18 technology?
- if no: show stopper!
- if yes: find range for W, L and operating current of a transistor (NMOS18 and/or PMOS18) or of a complementary parallel stage (improved power efficiency)

Answer: Drive requirements can be met!
The best possible power efficiency can be achieved with a push-pull stage
$L_{N,P}$ = 180nm, W_N*M_N = 50um, W_P*M_P = 175um
values depend on actual load
quiescent current can be lower than peak current (Class AB operation)
(see LTspice results)

Best possible drive capability if the channel is as short as possible

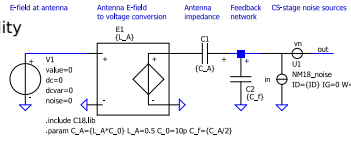






Step 2: can the active antenna be realized as a negative feedback amplifier?

The best performance-to-cost ratio can be obtained with negative feedback amplifiers.
The performance parameters of such amplifiers can be designed with a maximum orthogonality



Answer: True:
1. If a feeback configuration exists for which the impact of the feedback network on the
   - noise performance
   - drive capability
   does not affect the feasibility
2. If the gain accuracy, the bandwidth and the weak nonlinearity requirements can be met, together with an acceptable frequency response

False:
- If the above cannot be acieved, one could evaluate the feasibility of a cascade connection of amplifiers.

Design of the feedback configuration

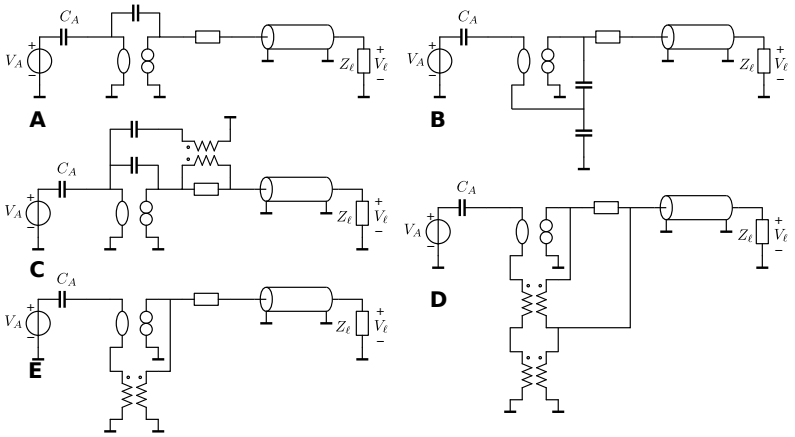
The amplifier configuration and the impact of feedback network(s) on noise performance and drive limitations

50Ohm output impedance: $\frac{B}{A} = 50,\ C = D = 0$

$\frac{D}{C} = 50,\ A = B = 0$

Infinite input impedance, antenna voltage sensing: $A = 0.5,\ B = 100$

Zero input impedance, antenna current sensing; antenna=linear impedance, no preference for voltage or current sensing: $C = \frac{sC_A}{2},\ D = 25sC_A$



Selection criteria:

Influence of ESD protection on device on weak nonlinearity

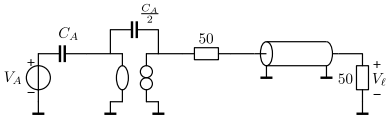
Influence of feedback network and brute-force impedances on noise performance

Influence of feedback network and brute-force impedances on drive capability

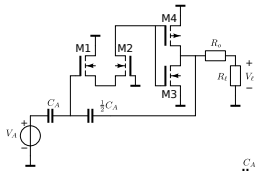
Influence of feedback network and brute-force impedances on power efficiency

Component availability (transformers)

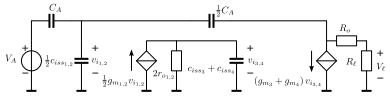
Selected:



Integrating transimpedance with brute-force 50Ohm output resistance



Signal path diagram with two-stage controller



Small-signal equivalent circuit with two-stage controller

Controller design

Number of stages and type of stages

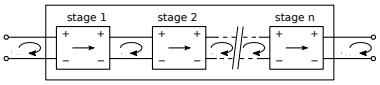
Best orthogonality between noise addition and drive capability:
- CS stage or balanced version

Largest bandwidth with lowest number of stages:
- All poles must be dominant
- Achievable MFM bandwidth is the n-th root of nth-order LP product.
- Use cascoded CS stage, or a balanced version of it

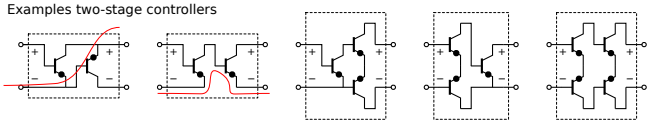
Low weak nonlinearity:
- Stages with low differential-error-to-gain ratio
- Servo differential-error-to-gain ratio is that of the loop gain divided by the loop gain
- Use CS stage, or a balanced version of it

Low static inaccuracy with lowest number of stages
- High DC loop gain
- Servo static inaccuracy is reciprocal value of DC loop gain
- Use cascode stage with high input impedance and high output impedance, or a balanced version of it

Interconnection of stages



Examples two-stage controllers



No port isolation.
Can only be used in combination with a transformer connected to one of the ports.

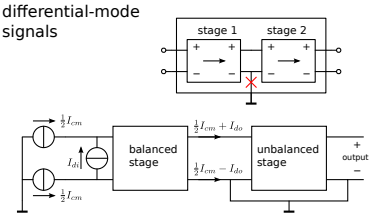
Simple two-transistor controller. Input current of the second stage flows through the external network.

Two-stage controller with anti-series output stage.

Two-stage controller with anti-series input stage. A push-pull stage can be used for the second stage.

Fully balanced two-stage controller.

Minimize conversion of common-mode into differential-mode signals



Interconnection of controller and feedback network

There exist two different connections between four-terminal controllers and their external network