Amplifier stages with discrete transistors

Basic CE and CS stages

NPN BJT

$V_{CE} > V_{CEsat}$

$V_{BE} > 0$

$I_C = I_s \left(\exp \frac{V_{BE}}{V_T}\right)\left(1 + \frac{V_{CE}}{V_A}\right)$

$I_B = \frac{I_C}{\beta_{DC}}$

N channel MOS

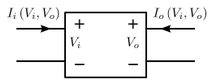
$V_{DS} > V_{sat} \quad V_{sat} = V_{GS} - V_t$

$V_{GS} > V_t$

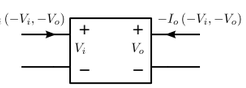
$I_D = \beta (V_{GS} - V_t)^2 (1 + \lambda V_{DS})$

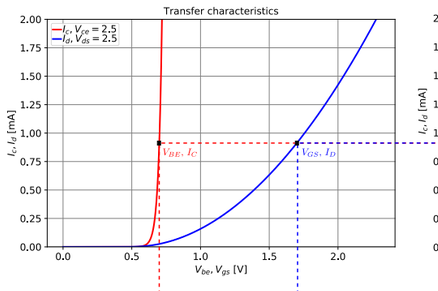
$I_G = 0$

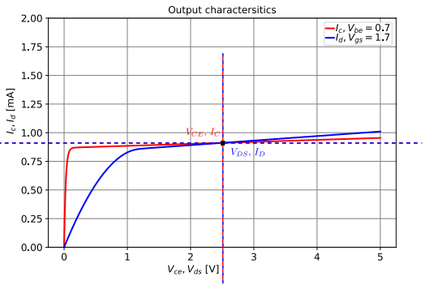
Voltage-controlled notation of a nonlinear two-port:

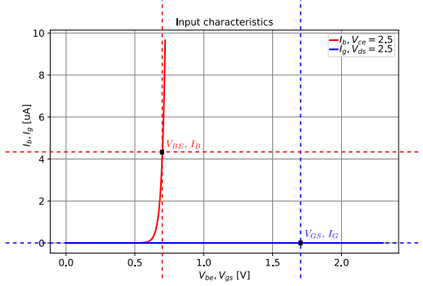


age-controlled notation of the complementary two-port:

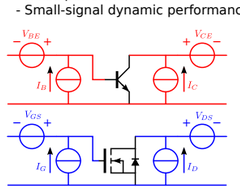








For processing bipolar signals:
- Select operating point at output port:
  - Voltage and current drive capability
  - Noise performance
  - Small-signal dynamic performance



Create zero bias conditions for the external circuitry by adding bias sources at both the input port the output port.

Schematic symbol of a biased transistor

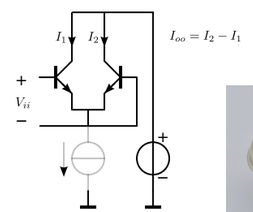
Balanced stages

Obtain odd transfer characteristics
- compensation of offset
- reduction of even-order nonlinearity

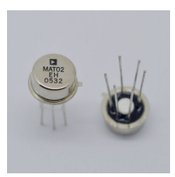
Improvement of port isolation
- Four-terminal stages
- Natural two-port approximation

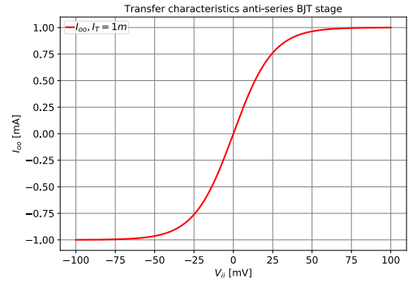
Implementation techniques
- Anti-series connection
- Complementary-parallel connection

Anti-series stage

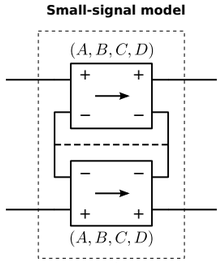


Compressing (limiting) voltage-to-current transfer

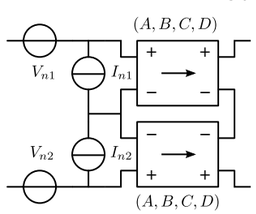




Small-signal model

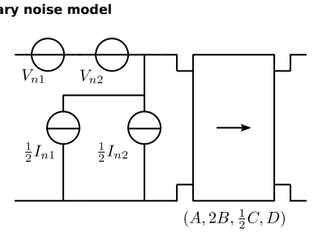


Stationary noise model



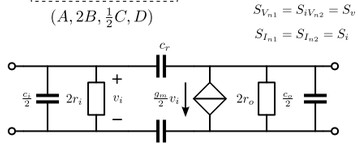
$S_{V_{n1}} = S_{iV_{n2}} = S_v$

$S_{I_{n1}} = S_{I_{n2}} = S_i$



$S_{(V_{n1}+V_{n2})} = 2S_v$

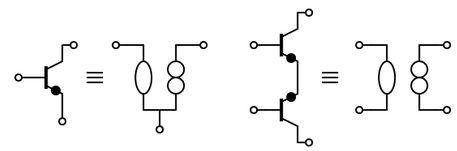
$S_{(\frac{1}{2}I_{n1}+\frac{1}{2}I_{n2})} = \frac{1}{2}S_i$



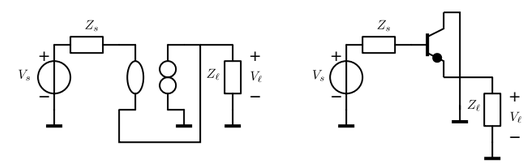
Consider behavioral modifications of the CE and the CS stage as the result of the application of balancing techniques.

Local feedback stages

Biased transistor: the simplest implementation of the nullor

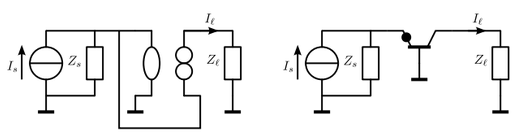


CC-stage (BJT) of CD stage (FET):
Nonenergic, non-inverting, unity-gain, negative feedback voltage amplifier (voltage follower)

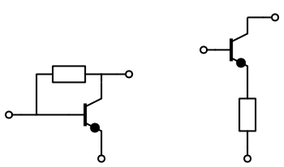


Use asymptotic-gain feedback model to evaluate the effect of feedback:
See example capacitively loaded CC-stage with 2N3904.

CB-stage (BJT) of CG stage (FET):
Nonenergic, non-inverting, unity-gain, negative feedback current amplifier (current follower)



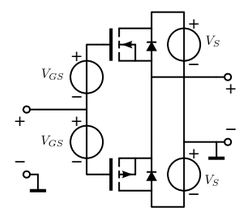
Passive single-loop
negative feedback stages:
- Series stage
- Shunt stage



Consider behavioral modifications of the CE and CS stage as the result of the application of negative feedback and/or balancing techniques.

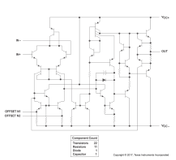
High loop gain:
Large change of the behavior compared with the basic stage:
- Improved accuracy
- Decreased weak nonlinearity
- Increased bandwidth
- Series feedback at a port: increased port impedance
- Parallel feedback at a port: decreased port impedance
- Noise as with feedback amplifiers: input referred noise sources: at best equal to those of basic stage
- Drive capability, power efficiency and energy storage as with feedback amplifiers: at best equal to those of basic stage

Combination of balancing and negative feedback



Complementary-parallel CD output stage

\+ Relatively easy to bias
\- No rail-to-rail output (low power efficiency) when driven from a rail-to-rail input
\- Unity gain.

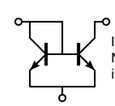


Indirect feedback stages

Indirect sensing:
Sence a copy of the load quantity

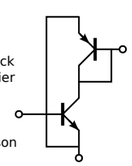
Indirect comparison:
Compare feedback quantity with a copy of the source quantity

Current mirror:
Inverting, indirect feedback unity-gain current amplifier



Indirect current sensing
No increase of output impedance

Voltage mirror:
Inverting, indirect feedback unity-gain voltage amplifier



Indirect voltage comparison
No increase of input impedance

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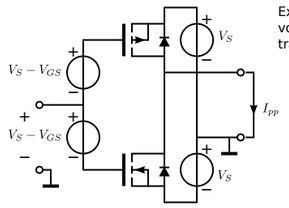
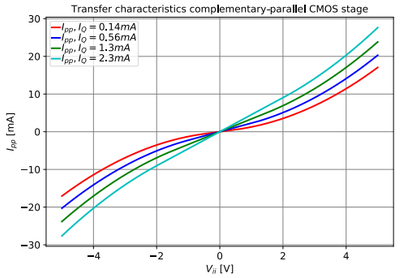
https://www.analog-electronics.eu

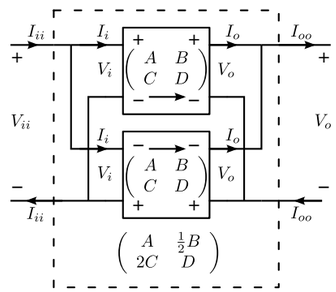
Complementary-parallel stage

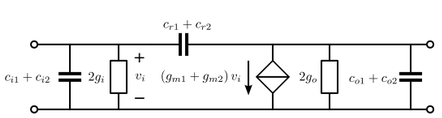


Expanding voltage-to-current transfer

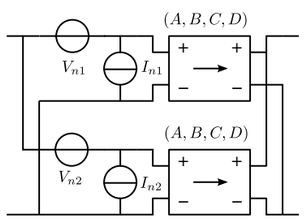


Small-signal model



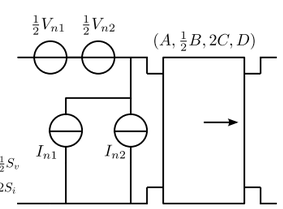


Stationary noise model



$S_{V_{n1}} = S_{iV_{n2}} = S_v$

$S_{I_{n1}} = S_{I_{n2}} = S_i$

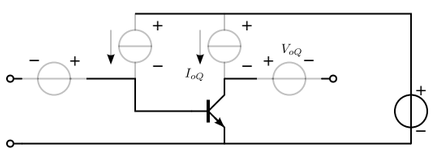


$S_{(\frac{1}{2}V_{n1}+\frac{1}{2}V_{n2})} = \frac{1}{2}S_v$

$S_{(I_{n1}+I_{n2})} = 2S_i$

Implementation of biasing: redirect current sources over the power supply

Example with grounded device and single supply:



I_{oQ} Determines maximum positive (sourcing) output current.

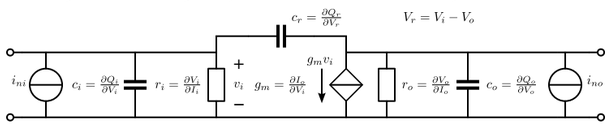
V_{oQ} Determines maximum negative (sinking) output cvoltage.

Voltage sources (level shifts):
- Absorbed in external circuitry
- Replace with capacitors (AC coupling)
- Implemented with current sources and (nonlinear) resistors

Temperature stability and sensitivity for device tolerances
Use error-reduction techniques to improve the accuracy of the biasing:
- Negative feedback biasing (if frequencies of interest to not include zero)
- Auto-zero techniques
- Compensation techniques

Current sources implemented with:
- Voltage reference and low-noise transadmittance amplifiers
- Replace with inductors (AC coupling)
- Implemented with (nonlinear) resistors

Modeling of the small-signal dynamic behavior and stationary noise behavior in the operating point.



Relate small-signal parameters to device parameters and operating conditions

BJT

$r_i = \frac{\beta_{AC}}{g_m}$

$g_m = \frac{I_C}{V_T}$

$r_o = \frac{V_{CE}+V_A}{I_C}$

$c_i = \frac{I_C}{V_T}\tau_F + C_{JE}$

$c_r = C_{JC}$

$S_{i_{ni}} = 2qI_B$

$S_{i_{no}} = 2qI_C$

$\beta_{AC} = \frac{\partial I_C}{\partial I_B}$ = small-signal current gain

τ_F = forward transit time

C_{JC} = collector-base junction depletion capacitance

C_{JE} = emitter-base junction depletion capacitance

MOS

$r_i = \infty$

$g_m = 2\sqrt{\beta I_D}$

$r_o = \frac{1}{\lambda I_D}$

$c_i = \frac{2}{3}C_{OX}$

$c_r = C_{DG}$

$c_o = C_{DB} + C_{SB}$

$S_{i_{ni}} = 2qI_G$

$S_{i_{no}} = 4kT\frac{2}{3}g_m$

C_{OX} = oxide capacitance

C_{DG} = drain-gate overlap capacitance

C_{DB}, C_{SB} = drain-bulk and source-bulk junction capacitances, respectively

Bulk resistances are omitted add base resistance for BJT (with associated noise)

Output capacitance only present in bulk-source connected MOS transistors.

Figure Of Merit

Unity-gain frequency of the small-signal current gain

$f_T = \frac{1}{2\pi}\frac{g_m}{c_i + c_r}$

T1 matrix parameters

$\mu = \frac{1}{A} = -g_m r_o \frac{1 - s\frac{c_r}{g_m}}{1 + sr_o(c_r + c_o)}$

$\zeta = \frac{1}{C} = -g_m r_i r_o \frac{1 - \frac{sc_r}{g_m}}{1 + s(r_o(c_o + c_r) + r_i(c_i + c_r(1 + g_m r_o))) + s^2 r_i r_o (c_i c_o + (c_i + c_o)c_r)}$

$\gamma = \frac{1}{B} = -g_m \left(1 - s\frac{c_r}{g_m}\right)$

$\alpha = \frac{1}{D} = -g_m r_i \frac{1 - s\frac{c_r}{g_m}}{1 + sr_i(c_i + c_r)}$

Miller effect