Design of an active antenna for DAB receivers

Specification

Functional

The DAB receive signal (174-240MHz) is taken from a short rod antenna.
This signal should be amplified up to a level that it can be converted by an RF ADC.
In the frequency range of interest, the impedance of the short rod antenna can be represented by the series connection of a linear resistor (4Ohm) and a linear capacitor (4pF).
The peak open circuit voltage at the antenna output is 25mV.
The input impedance of the ADC equals 1pF, it has a single-ended input. Its full-scale input voltage is 0.5V_{pp}.

Performance

1. The spectral density of the noise at the input of the ADC should be less than 10nV/rt(Hz)
2. The bandwidth should be adequate and a flat frequency response is desired
3. The intermodulation distortion should be less than -80dB for input signal levels up to 20mV_p
4. The mid-band gain accuracy should be better than 20%

Environment

5. The operating temperature ranges from 0 to 70 deggrees Celsius

Cost Factors

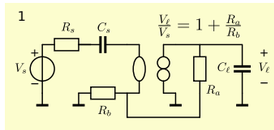
6. The amplifier should be realized in CMOS18 technology: fT_{max}=80GHz
7. The power dissipation should be less then 15mW
8. A temperature compensated low-noise current reference source of 0.1mA is available
9. The power supply voltage ranges from 1.75 to 1.85V

Discussion and interpretation of the specifications

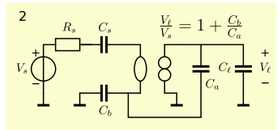
1. The spectral density of the source-referred noise should be less than 1nV/rt(Hz) Over the frequency range of interest this amounts to 8.12uV RMS total source-referred noise and 81.2uV ADC input noise.
2. The amplifier gain should be 20dB (10x), this maps the peak antenna output signal to the ADC input voltage range.
3. An intermodulation distortion test bench is not given, we will use two tones of 10mV peak with frequencies of 200 and 210 MHz and measure the IM3 levels
4. The peak load current amounts about 380uA (1pF, 240MHz, 250mV_p)
5. The maximum available supply current is about 8mA (1.85V, 15mW)

Design of amplifier type

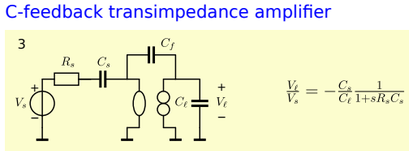
R-feedback voltage amplifier



C- feedback voltage amplifier



C-feedback transimpedance amplifier



Discussion and selection of the amplifier type

	1	2	3
noise	-	+	+
bandwidth	+	+	+
distortion	-	-	++
accuracy	+	+	-
power	-	+	+
complexity	-	-	+

Notes
1. The feedback resistors in amplifier 1 adversely affect the noise performance and the power efficiency
2. A possible nonlinear input capacitance of the controller adversely affects the distortion (ESD protection)
3. The accuracy of the gain of the transimpedance amplifier is limited by the tolerance of the capacitor
4. The transimpedance amplifier has less feedback elements and has, at this stage the lowest complexity

best score

Controller design

Design of the input stage

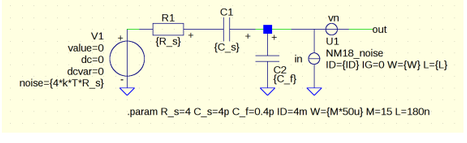
Noise design considerations

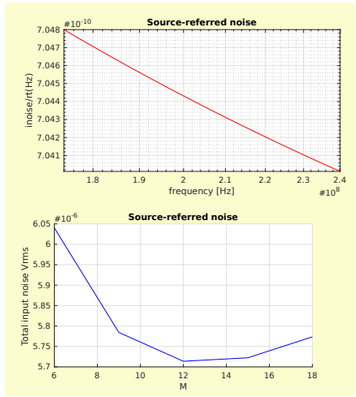
1. Input stage type: CS or balanced (minimum influence of noise of other stages)
2. A single stage input device requires less current for the same noise performance
3. As a starting point, we will assign half of the current budget for the input stage and the other half to the output stage, optimization can be done later.

SLiCAP noise model

SLiCAP schematic for design of the noise performance

- The influence of the feedback capacitance on the noise performance of the amplifier can be evaluated as if it is connected in parallel with the source.





Source-referred noise spectrum in V/rt(Hz) for an NMOS with:
- ID=4mA
- L=180nm
- W=50um
- M=15 (W_{eff}=750um)

Source-referred RMS noise for an NMOS with:
- ID=4mA
- L=180nm
- W=50um
- M=6...18 (W_{eff}=M*W)

Noise design conclusion

1. A current budget for the input transistor of about 4mA is OK
2. With this budget, the effective width may vary over a wide range. This leaves room for optimization at a later stage.
3. The transistor operates in moderate inversion for a low 1/f noise
4. With M=15 we have: IC=1.5, FT=7.8GHz, gm=64mS, Cgs=0.98pF and Cgs=225fF

Design of the output stage

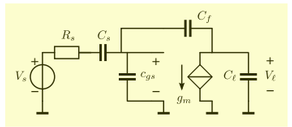
Load drive requirement considerations

1. The output stage should be a CS stage or its balanced version. If so preceeding stages minimally contribute to the distortion
2. The load drive requirement is about 600uA, (inclusing the current through Cf). This current can be delivered by the input stage: a single-stage solution may be possible.

Single-stage solution

Bandwith design considerations

1. The bandwidth of a single-stage solution is adequate if its loop gain poles product is equal or greater than the required low-pass cut-off frequency of the amplifier



Note
At this stage we will ignore the effect of the gate-drain capacitance and of the output resistance of the stage. These effects can be reduced by using a cascode stage.

The loop gain pole product of this single-stage solution is:

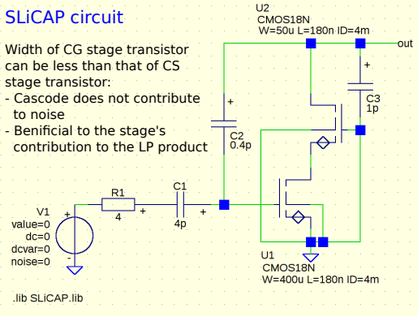
$$LP = \frac{1}{2\pi} \frac{C_f}{C_\ell + C_f} \frac{g_m}{s(C_{gs}+C_s)} = 560\text{MHz}$$

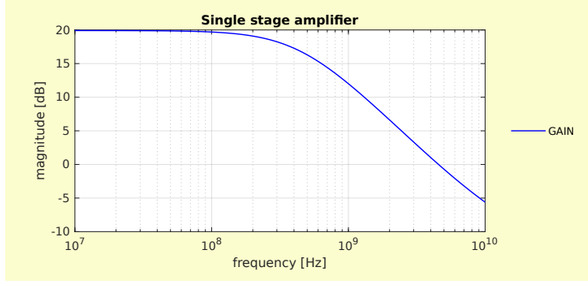
Note
The influence of R_s on the LP product can be ignored in the frequency band of interest.

The bandwidth of the single-stage solution appears to be OK.
We will check the results with a cascoded stage with both SLiCAP and SPICE.

SLiCAP circuit

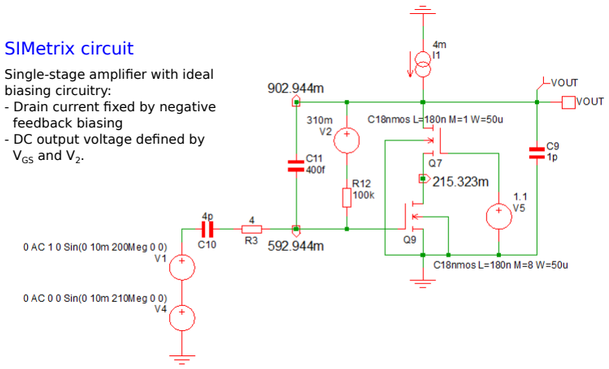
Width of CG stage transistor can be less than that of CS stage transistor:
- Cascode does not contribute to noise
- Beinficial to the stage's contribution to the LP product

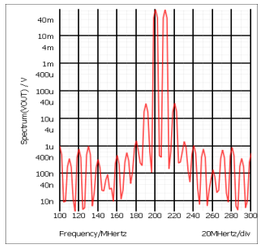


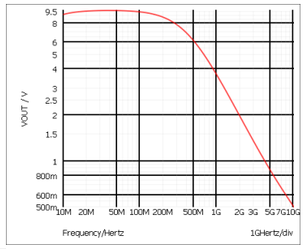


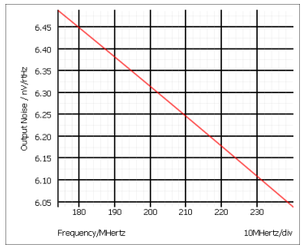
SIMetrix circuit

Single-stage amplifier with ideal biasing circuitry:
- Drain current fixed by negative feedback biasing
- DC output voltage defined by V_{GS} and V_2.









Bandwidth: PASS
Noise: PASS
IM3: FAIL
Supply power: PASS

Show-stopper single stage

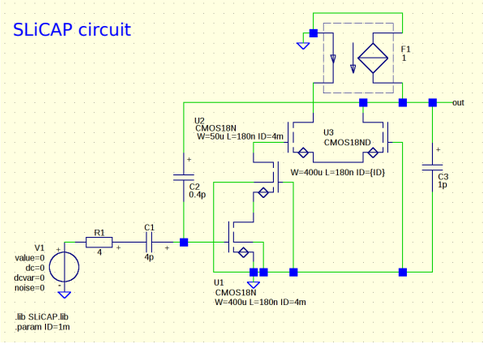
1. Implementation of the biasing will add an extra capacitance to the output node and reduce the loop gain:
   - distortion will increase
   - bandwith will reduce
2. Biasing circuitry will insert nonlinear resistors in the signal path:
   - distortion will increase

Two-stage solution

Aim is to reduce the distortion

- Keep the bias current of the output stage as low as possible
- Use a balanced stage, because it should be non inverting
- First design for stability in SLiCAP
- Then optimize for distortion in SPICE

SLiCAP circuit




```
No errors found!
    GAIN
    Unable to determine DC value!
    Poles:
              RealPart        ImagPart        Frequency       Q
              ________        ________        _________       ____

    p_1     4.0318e+07     -1.6687e+09     1.6692e+09     20.701
    p_2     4.0318e+07      1.6687e+09     1.6692e+09     20.701
    p_3      -1.427e+10              0      1.427e+10          0
    p_4     -6.0737e+10              0     6.0737e+10          0

    Zeros:
              RealPart        ImagPart        Frequency       Q
              ________        ________        _________       ____

    z_1      7.6855e+09              0     7.6855e+09          0
    z_2     -1.0763e+10      1.2798e+10     1.6722e+10    0.77684
    z_3     -1.0763e+10     -1.2798e+10     1.6722e+10    0.77684
```

Second-order
Bandwidth =1.67 GHz
Instable

Implement a phantom zero at the load:
- Resistor between out and the load (C3)
- Frequency 1.1GHz 0.5*sqrt(2)*Bandwidth

Phantom zero compensation at the load

- The resistor decouples the load capacitance from the amplifier which increases the number of poles
- The new pole is dominant and increases the order of the system
- The amplifier is stable but it does not have an MFM characteristic

```
    GAIN
    Unable to determine DC value!
    Poles:
              RealPart        ImagPart        Frequency       Q
              ________        ________        _________       ____

    p_1     -6.5431e+08      2.2355e+09      2.3293e+09     1.78
    p_2     -6.5431e+08     -2.2355e+09      2.3293e+09     1.78
    p_3      -1.638e+09              0       1.638e+09        0
    p_4     -1.3878e+10              0      1.3878e+10        0
    p_5     -7.3971e+10              0      7.3971e+10        0

    Zeros:
              RealPart        ImagPart        Frequency       Q
              ________        ________        _________       ____

    z_1      7.6855e+09              0     7.6855e+09          0
    z_2     -1.0763e+10      1.2798e+10     1.6722e+10    0.77684
    z_3     -1.0763e+10     -1.2798e+10     1.6722e+10    0.77684
```

Third-order
Bandwidth > 1GHz
Stable

Optimization in SPICE

- Now that the amplifier is stable and has a sufficiently large bandwidth, we can design the biasing
  This is done in steps:
  1. Use ideal bias sources, adjust operating point, frequency compensation and check the distortion
  2. Step-by-step implement the bias sources and adjust operating conditions, the frequency compensation and check the distortion.

Final results

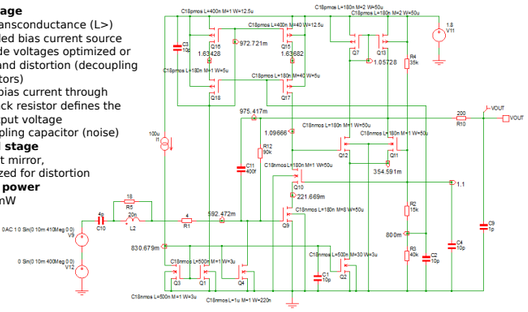
After optimization of the operating conditions and the frequency compensation

Biasing

First stage
- Low-transconductance (L>) cascoded bias current source
- Cascode voltages optimized or noise and distortion (decoupling capacitors)
- Small bias current through feedback resistor defines the DC output voltage
- Decoupling capacitor (noise)

Second stage
- Current mirror, optimized for distortion

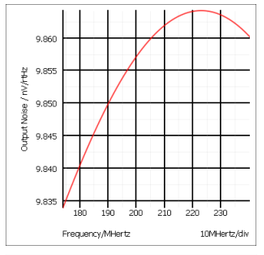
Supply power
- 12.73mW

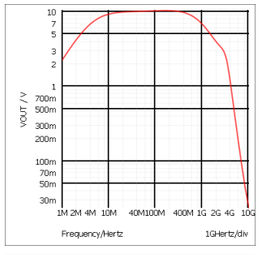


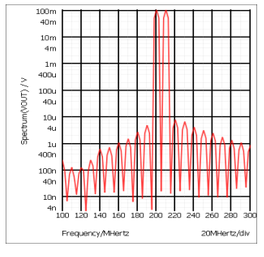
Frequency compensation

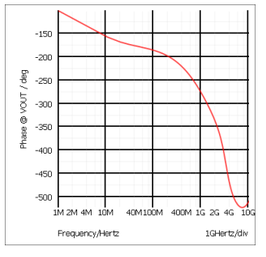
Phantom zero at the load
- The value of the phantom zero resistor is optimized for a flat response

Phantom zero bandwith limitation at the source
- The bandwidth of the compensated amplifier is much larger than required:
  - Out-of-band high-frequency interference may yield in-band IM components
  - Limiting of the bandwidth is desired
  - Bandwith limitation with a phantom zero at the input is the best technique (if noise performance degradation can be kept within acceptable limits):
    - Interference signals are attenuated before entering the amplifier
    - The out-of-band loop gain is increased, which reduces the distortion









notes
1. Graphs are for nominal power supply and T=27 deg Celsius.
2. The BSIM CMOS18 model parameters are for educational purpose only:
   - no process corner parameter sets
   - device widh up to about 50um
   - device multiplier M for wider devices

Bandwidth: PASS
Noise: PASS
IM3: PASS
Supply power: PASS