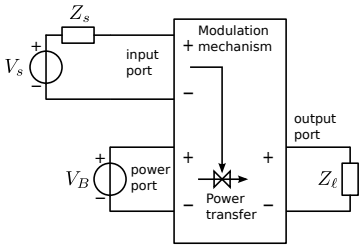
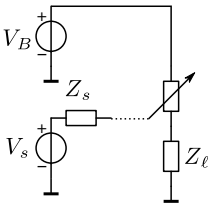
Principle of Amplification and Biasing

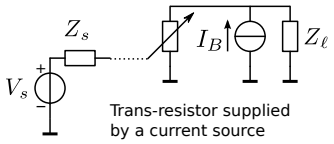
Principle of Amplification

Modulation of power transfer from power source to the load by the signal source



Trans-resistor supplied by a voltage supply





Trans-resistor supplied by a current source

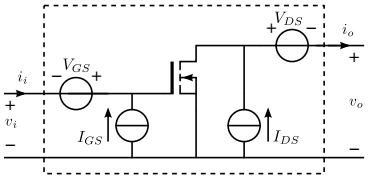
Principle of Biasing

Add power sources such as to obtain the best possible approximation of a linear transfer.

- Input v-i characteristic passes through the origin
- Output v-i characteristic passes through the origin

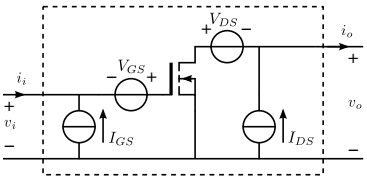
As a result all transfer characteristics (A, B, C, D) pass through the origin.

Biased CS stage: four possible arrangements



Biased amplifier stage - 1

Bias power delivered by I_{GS} and I_{DS}



Biased amplifier stage - 2

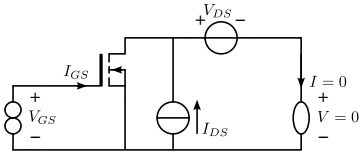
Bias power delivered by V_{GS} and V_{DS}

Determination of the bias voltages and currents

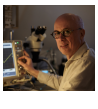
Two of the four sources can be selected independently The other two follow from the selected ones and the device equations.

The output port bias sources determine the stage's drive capability:

- VDS: maximum negative output voltage excursion
- IDS: maximum positive output current excursion



Circuit for finding the input port bias quantities for a device and its desired output port operating point



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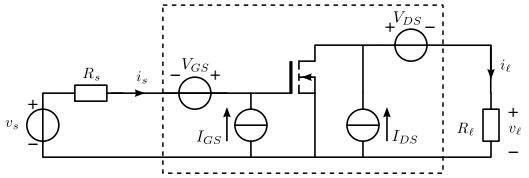
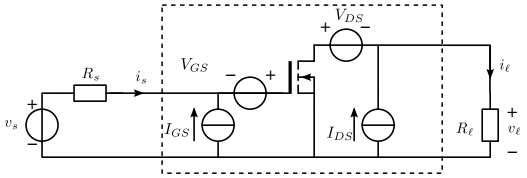
Biased amplifier stage

Arrangement with no current through the bias voltage sources.



Biased amplifier stage, no current through voltage sources

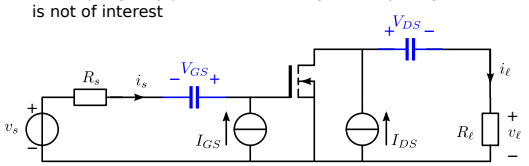


Biased amplifier stage, no voltage across current sources

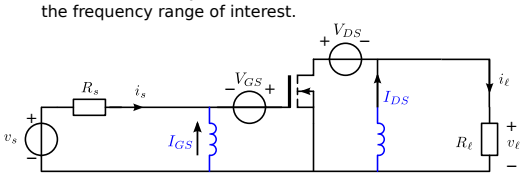
AC coupling

AC coupling is always required if no DC current is allowed through source and/or load or no DC voltage is allowed across it

AC coupling only possible if zero (signal) frequency (DC) is not of interest



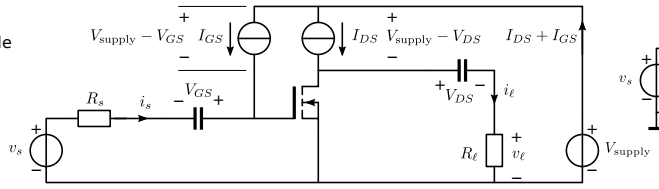
Impedances in series with the signal path, and admittances in parallel with the signal path should be relatively small over the frequency range of interest.



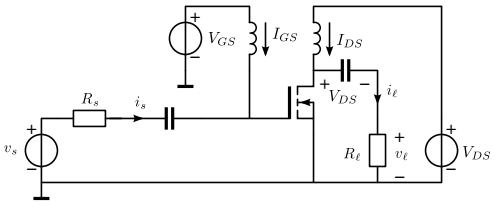
Biasing with power supply and passive elements

Add a power supply voltage and redirect the current sources such that:

Voltage supply source is the only bias source that delivers power (product V and I negative)

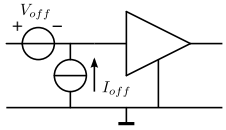


Resulting sources can be realized with passive elements (product V and I positive)



Biasing errors

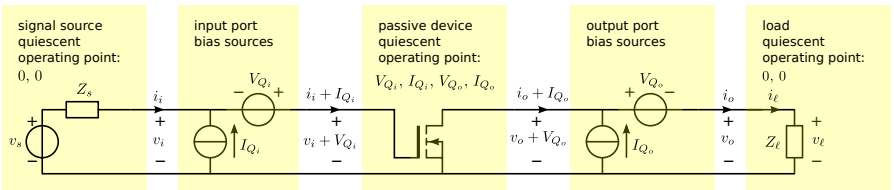
- Transistor characteristics depend on temperature and change over time
- Implementation of bias voltages and currents has limited accuracy
- Remaining errors can be modeled as noise sources
- Design friendly representation with equivalent-input error sources:
  - Equivalent-input offset current
  - Equivalent-input offset voltage

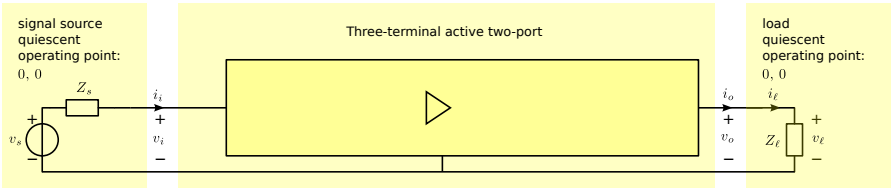


Bias error reduction

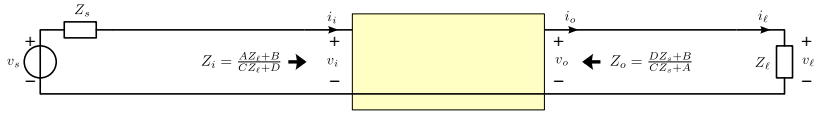
- Biasing errors can be kept small through application of error-reduction techniques:
  - Compensation
  - Negative feedback
  - Auto-zero

Small-signal model of a biased stage





Small-signal equivalent network



Transmission matrix -1 (anti-causal) representation

$$\begin{pmatrix} v_i \\ i_i \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} v_o \\ i_o \end{pmatrix}$$

Maximum low-frequeny available power gain: $G_{P_{max}} = \frac{1}{4AD}$

Z_s, A, B, C, D: Real
$Z_i = Z_s$: imput power matching
$AD = BC$: unilateral