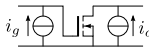# CS stage Noise Design

MOS noise model

Biased CS stage with intrinsic noise sources

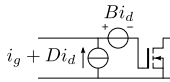

$$S_{id} = 4kTn\Gamma g_m \left(1 + \frac{f_\ell}{f}\right)$$

$$S_{ig} = 2qI_G$$
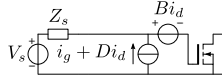
$$f_\ell = \frac{\pi KF}{3kTn\Gamma} f_T = \alpha f_T$$
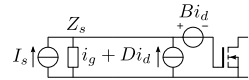
$$B = -\frac{1}{g_m}$$

$$D = -\frac{s}{\omega_T}$$

Biased CS stage with equivalent-input noise sources

CS stage driven from a voltage source

$$S_{vs} = S_{id}|B + DZ_s|^2 + S_{ig}|Z_s|^2$$

CS stage driven from a current source

$$S_{is} = S_{id}|BY_s + D|^2 + S_{ig}$$

Correlation between both sources needs to be accounted for.

$$v_n^2 = \int_{f_{min}}^{f_{max}} 4kTR_s \left(1 + \left(\frac{n\Gamma}{g_m R_s} + g_m R_s n\Gamma \frac{f^2}{f_T^2}\right)\left(1 + \frac{\alpha f_T}{f}\right)\right) df$$

$$g_m = 2\pi f_T c_{iss}$$

$$v_n^2 = 4kTR_s \int_{f_{min}}^{f_{max}} \left(1 + n\Gamma\left(\frac{1}{2\pi f}\frac{\alpha}{R_s c_{iss}} + \frac{1}{R_s g_m} + 2\pi f c_{iss}\alpha R_s + g_m R_s \frac{f^2}{f_T^2}\right)\right) df$$

Procedure for finding the best noise performance:

1. Lowest RMS value:

   Write g_m, f_T and c_{iss} as a function of IC, W, L. Find a solution that satisfies the requirements (partial derivatives)

2. Lowest floor noise:

   Short and wide channel operating in high inversion:

   $$S_{v,floor} = 4kTR_s\left(1 + \frac{n\Gamma}{R_s g_m}\right)$$
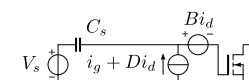
3. Low level of 1/f noise:

   Large input capacitance:

   $$S_{v,\frac{1}{f}} = \frac{2kTn\Gamma\alpha}{\pi c_{iss}}\frac{1}{f}$$

4. Low level of high-frequency noise (gate-induced noise)

   Short and narrow channel operating in high inversion (low transconductance, high cut-off frequency):

   $$v_n^2 = 4kTn\Gamma g_m R_s^2 \left(\frac{\alpha f}{f_T} + \frac{f^2}{f_T^2}\right)$$

CS stage driven from a capacitive voltage source

$$S_{vs} = 4kTn\Gamma g_m \left|-\frac{1}{g_m} - \frac{jf}{f_T}\frac{1}{j2\pi f C_s}\right|^2 \left(1 + \frac{\alpha f_T}{f}\right)$$

$$S_{vs} = \frac{4KTn\Gamma}{g_m}\left(1 + \frac{c_{iss}}{C_s}\right)^2\left(1 + \frac{\alpha f_T}{f}\right) = \frac{4KTn\Gamma}{2\pi f_T c_{iss}}\left(1 + \frac{c_{iss}}{C_s}\right)^2\left(1 + \frac{\alpha f_T}{f}\right)$$

Optimum if $c_{iss} = C_s$

$$S_{vs} = \frac{16kTn\Gamma}{g_m}\left(1 + \frac{\alpha f_T}{f}\right) = \frac{16kTn\Gamma}{g_m}\left(1 + \frac{\alpha g_m}{2\pi f C_s}\right) = S_{floor}\left(1 + \frac{f_\ell}{f}\right)$$

Design equation g_m:

$$\frac{16kTn\Gamma}{S_{v,floor}} \le g_m \le f_\ell \frac{2\pi C_s}{\alpha} \qquad \alpha = \frac{KF\pi}{3kTn\Gamma}$$

Solution if:

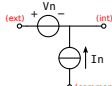$$\frac{8}{S_{v,floor}} < f_\ell \frac{3C_s}{KF}$$

If not: SHOW STOPPER

Or:

$$\text{technology Parameter} \rightarrow \quad \frac{8}{3}KF < S_f f_\ell C_s \quad \leftarrow \text{Application requirements}$$
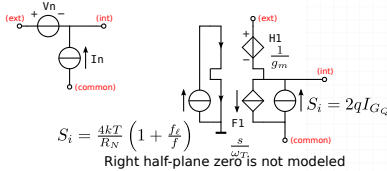
Active antenna input MOS

Biased CS stage

Antenna conversion length: 0.5m
Antenna conversion gain: 0.5m
Antenna E-field reffered noise: see application description.
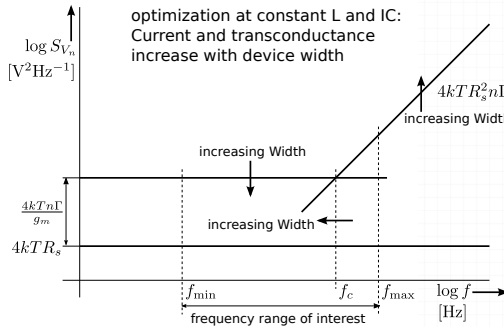
SLiCAP MOS noise model

Symbol

Subcircuit

$$S_i = \frac{4kT}{R_N}\left(1 + \frac{f_\ell}{f}\right) \qquad S_i = 2qI_{GQ}$$

Right half-plane zero is not modeled

Design of noise performance

CS stage driven from a resistive source

$$S_v = 4kTR_s\left(1 + \left(\frac{n\Gamma}{g_m R_s} + g_m R_s n\Gamma \frac{f^2}{f_T^2}\right)\left(1 + \frac{\alpha f_T}{f}\right)\right)$$

optimization at constant L and IC:
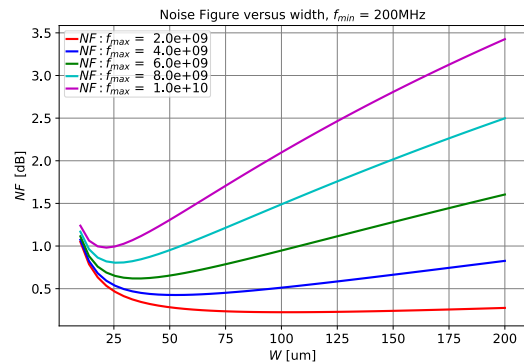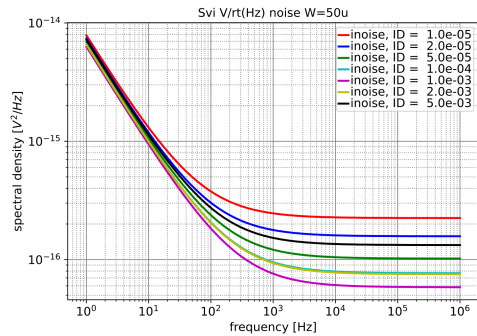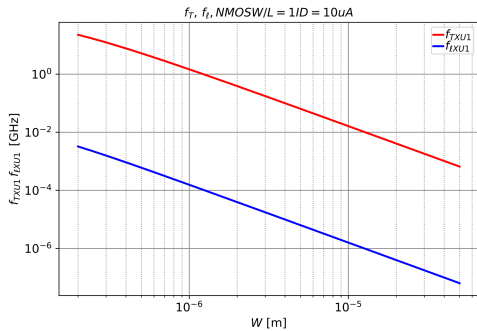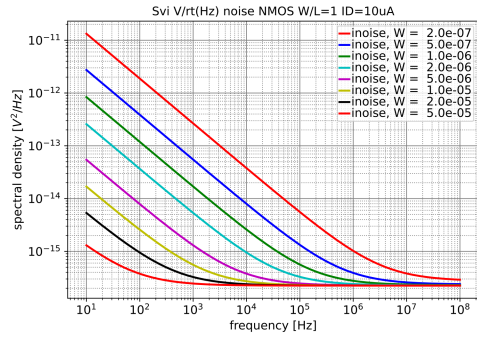Current and transconductance increase with device width

$4kTR_s^2 n\Gamma g_m \frac{f^2}{f_T^2}$ increasing Width

increasing Width

increasing Width

frequency range of interest

IF Conflicting requirements THEN SHOW STOPPER

Other source types

Similar procedure, different conclusions.

Design equations

Relations between performance parameters, cost factors and design parameters.

specified
specified
specified
specified

Voltage noise NMOS

Svi V/rt(Hz) noise NMOS W/L=1 ID=10uA

f_T, f_ℓ, NMOS W/L = 1 ID = 10uA

Svi V/rt(Hz) noise W=50u

Noise Figure versus width, f_{min} = 200MHz