Structured Amplifier Design in CMOS technology

Hierarchically structured circuit design process for amplifiers and bias sources

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Design data accumulates
with every design step

Application description
with initial specification

Specification

Performance		Noise / zero error / drift Signal power Linearity
Costs		Chip area Supply power
Environment		Temperature EMI
Safety		ESD
Reliability		

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Object Performance Specification
Object Test Specification
Figure of merit

Concept design

Type		Port impedances (differential-mode, common-mode)
Structure		Cascade connection of amplifiers Parallel / series connections of amplifiers or sources

Child hierarchical level

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Application description
and initial specification of
each amplifier or bias source

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Feedback configuration of single amplifier
or DC bias source
including over-all biasing concept

Signal path design

Output stage	Drive capability		Type Geometry (W, L) Drive requirements
Input stage	Noise performance DC reproducibility		Type Geometry (W, L) Operating point
Number of stages	Accuracy, bandwidth, and distortion		Mid-band loop gain LP product diff. error to gain ratio
Interconnection of stages	Accuracy, bandwidth, distortion, and biasing complexity		Type of stages Geometry (W, L) Operating point Interconnection
Frequency compensation	Frequency stability Filter characteristic		Type of compensation Implementation

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Most promising
signal path

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Most promising
amplifier circuit

Biasing concept design

Minimization of floating
voltage sources

Combination of current sources

DM and / or CM feedback loops

Child hierarchical level

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Application description
and initial specification
of each bias source

Performance verification

Execution of tests from Object Test specification

Performance parameters Cost factors to be optimized	Design Parameters for optimization
FOM	Geometry of MOS transistors Operating point of MOS transistors Values of passive components

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Performance optimization plan

Performance optimization

Execution of performance optimization plan

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Amplifier circuit with
optimized performance