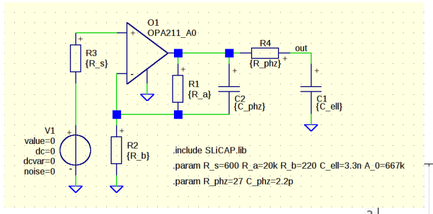
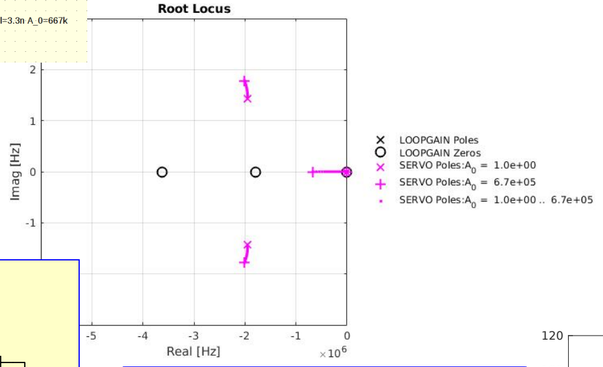
EE3C11: Structured Electronic Design
My First Voltage Amplifier
Design example EE3C11





SLiCAP project: myFirstVamp

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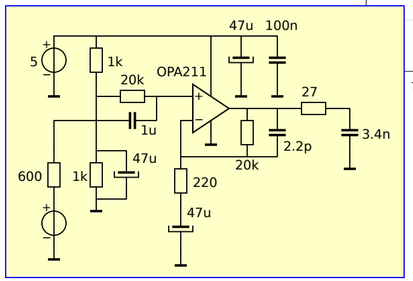
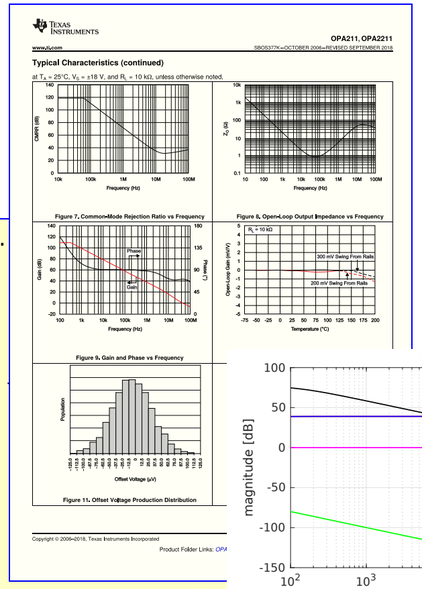
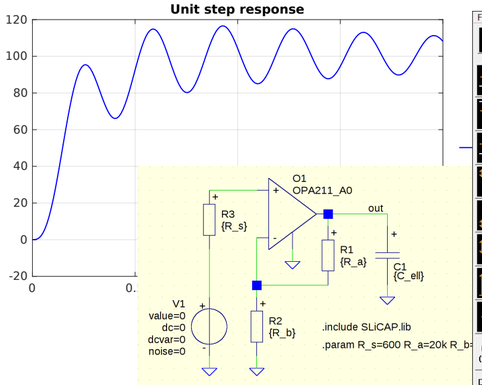
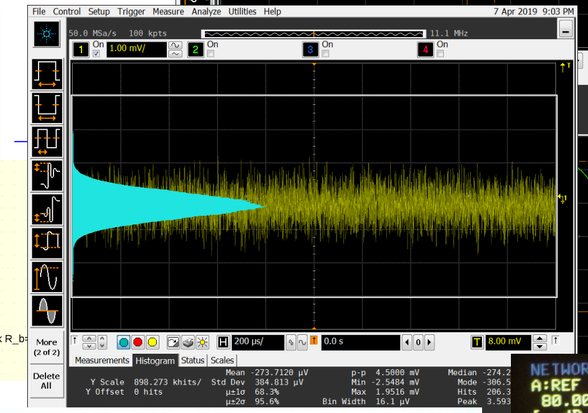
SLiCAP: Symbolic Linear Circuit Analysis Program, Version 0.6 © 2009-2019 Anton Montagne

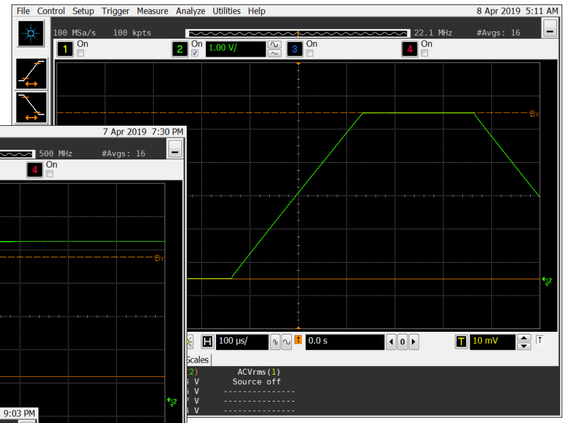
For documentation, examples, support, updates and courses please visit: analog-electronics.eu

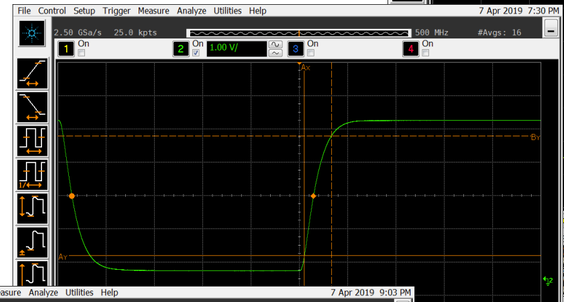


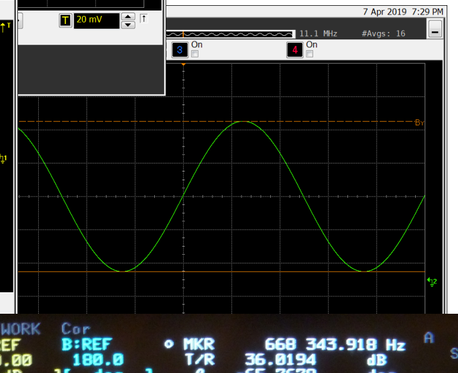


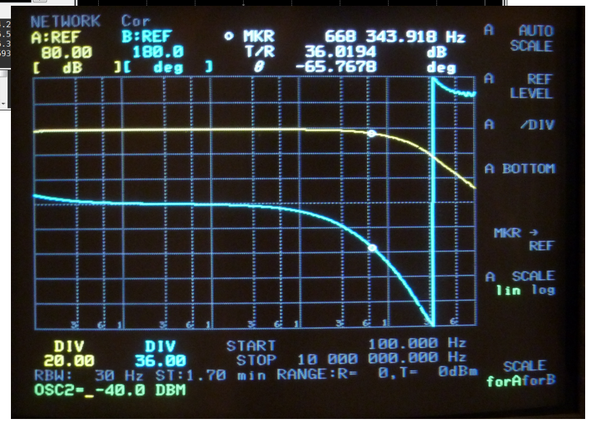










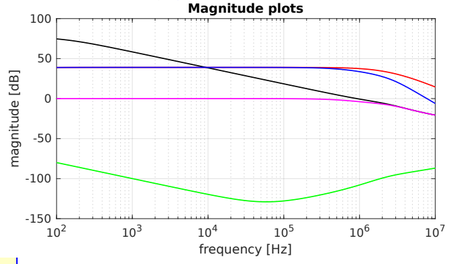


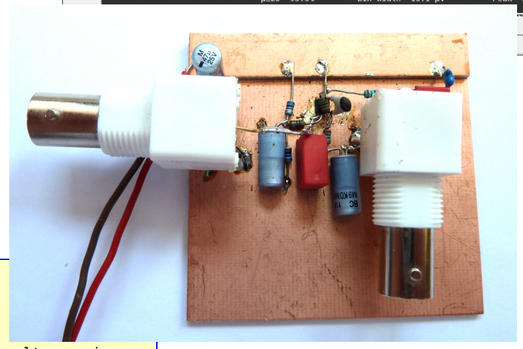

```
Checking circuit: myFirstVampCompensated.
No errors found!
    GAIN
    DC value = 9.189e+01
    Poles:
```

	RealPart	ImagPart
p_1	-7.8738e+05	0
p_2	-1.6015e+06	1.9166e+06
p_3	-1.6015e+06	-1.9166e+06
p_4	-1.9604e+07	0
p_5	-2.383e+07	0
p_6	-5.0504e+08	0

Zeros:

	RealPart	ImagPart	Frequency	Q
z_1	-1.061e+07	0	1.061e+07	0
z_2	-3.9963e+07	0	3.9963e+07	0
z_3	-8.0941e+08	-7.4266e+08	1.0985e+09	0.67858
z_4	-8.0941e+08	7.4266e+08	1.0985e+09	0.67858





```
.model OPA211_A0 OV
+ cd = 8p  ; differential-mode input capacitance
+ gd = 50u ; differential-mode input conductance
+ cc = 2p  ; common-mode input capacitance
+ av = {A_0*(1+s/2/PI/40M)/(1+s/2/PI/120)/(1+s/2/PI/20M)}   ; voltage gain
+ zo = {3.6k/(1+s*3.6k*8u) + 0.7 + s*900n*60/(60+s*900n)}   ; output impedance
```