Design of application-specific amplifiers with OpAmps

Structured design approach

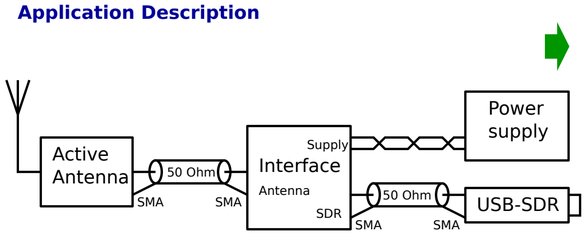
- Benefits
  - First time right
  - Predictable results
  - Manageble design process
  - Guaranteed by design
  - Knowledge building

- Features
  - Clear distinction between concepts and implementation
  - SLiCAP: Python based integrated design and HTML documentation tool
  - Use dedicated models for specific performance aspects during various stages of the design

- Practical approach:
  1. Specification of performance, environment and costs
  2. Concept development
  3. Implementation study (technology and components)
  4. Circuit engineering
  5. Design verification (simulation, prototype, ...)
  6. Design documentation (design, production, test, ...)

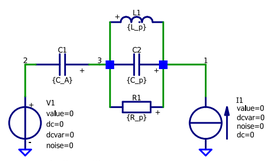
- Clear theoretical basis:
  - Physics
  - Signal processing
  - Control theory
  - Network theory
  - Systems engineering

Application Description

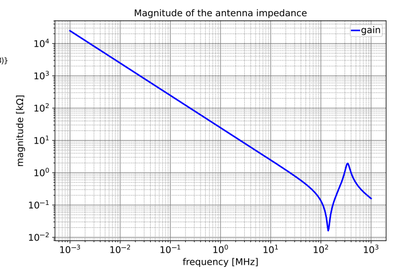


Application data:
- Antenna length: 0.5m
- Frequency range: 10kHz - 30MHz
- E-field at antenna: 0.45V_{rms}/m
- Output signal: 0dBm @ 50Ohm
- Power supply voltage: 7V
- Power dissipation < 250mW

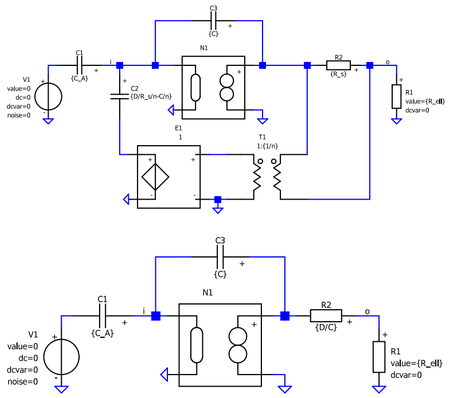
Source modeling




```
.param P1={log(2*i/r, 10)}
.param C_A={2*12.0674*L*1p/(P1-0.7245)}
.param C_p={4p*L*(0.89075/(P1^0.8006-0.861)+0.02541)}
.param L_p={0.1u*L*((1.4813*P1)^1.012+0.6388)}
.param R_p={1k*(0.41288*P1^2+7.4075*(2*L/r)^-0.02389-7.27408)}
.param L=0.5 r=0.0025
```



Concept development



Implementation study

ANALOG DEVICES

Low Noise, 1 GHz *FastFET* Op Amps

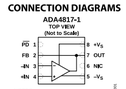
Data Sheet ADA4817-1/ADA4817-2

FEATURES
- High speed
  - −3 dB bandwidth (G = 1, R_L = 100 Ω): 1050 MHz
  - Slew rate: 870 V/µs
  - 0.1% settling time: 9 ns
- Input bias current: 2 pA typical
- Input capacitance
  - Common-mode capacitance: 1.3 pF typical
  - Differential mode capacitance: 0.1 pF typical
- Low input noise
  - Voltage noise: 4 nV/√Hz at 100 kHz
  - Current noise: 2.5 FA/√Hz at 100 kHz
- Low distortion: −90 dBc at 10 MHz (G = 1, R_L = 1 kΩ)
- Linear output current: 40 mA
- Supply quiescent current per amplifier: 19 mA typical
- Powered down supply quiescent current per amplifier: 1.5 mA typical

APPLICATIONS
- Photodiode amplifiers
- Data acquisition front ends
- Instrumentation
- Filters
- ADC drivers
- Output buffers

CONNECTION DIAGRAMS

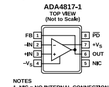
ADA4817-1
TOP VIEW
(Not to Scale)



NOTES
1. NC = NO INTERNAL CONNECTION.

Figure 1. 8-Lead LFCSP (CP-8-13)

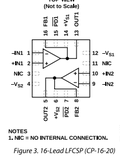
ADA4817-1
TOP VIEW
(Not to Scale)



NOTES
1. NC = NO INTERNAL CONNECTION.

Figure 2. 8-Lead SOIC (RD-8-1)

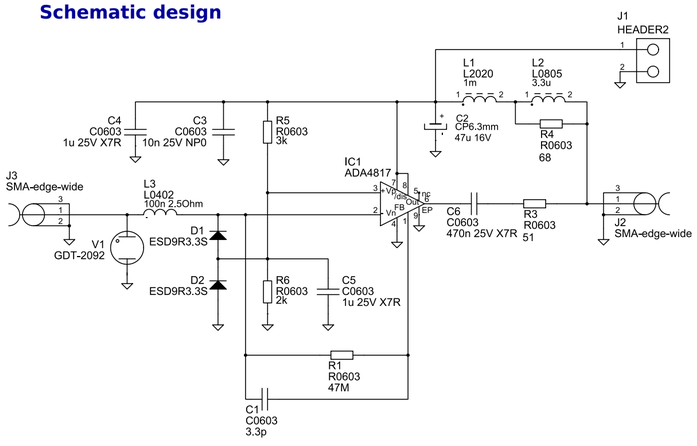
ADA4817-2
TOP VIEW
(Not to Scale)



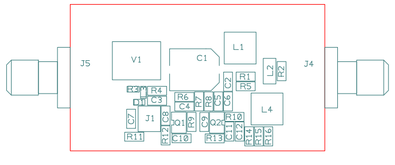
NOTES
1. NC = NO INTERNAL CONNECTION.

Figure 3. 16-Lead LFCSP (CP-16-20)

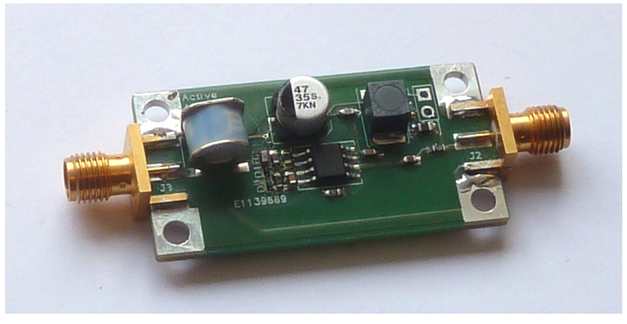
Schematic design

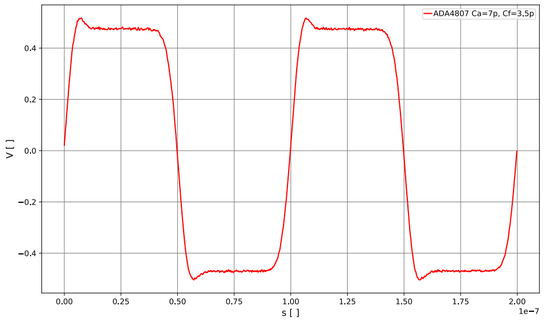


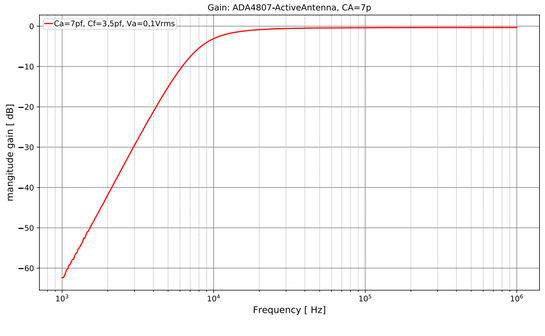
PCB design

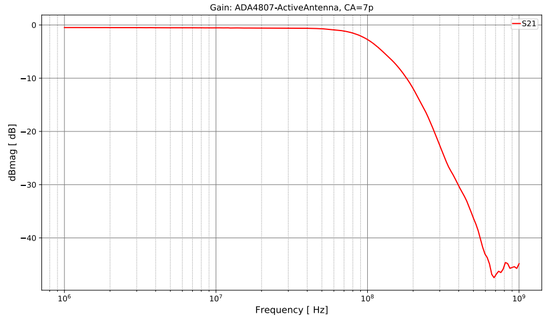


Assemby and test









ESD9R3.3S, SZESD9R3.3S

ESD Protection Diode
Ultra−Low Capacitance

The ESD9R is designed to provide ESD protection for ASSPs and ASICs used in ultra low current applications such as human body sensors. These devices have been designed for leakage under 1 nA from 0°C to 50°C when turned off. During an ESD event, these devices turn on to clamp the ESD to a safe voltage level for the IC. These devices have the added benefits of low capacitance for high speed data lines and small package size for space constrained designs.

Specification Features:
- Ultra−Low Leakage < 1 nA
- Ultra−Low Capacitance 0.5 pF
- Low Clamping Voltage
- Small Body Outline Dimensions: 0.039" x 0.024" (1.00 mm x 0.60 mm)
- Low Body Height: 0.016" (0.4 mm)
- Stand−off Voltage: 3.3 V
- Response Time < 1.0 ns
- IEC61000−4−2 Level 4 ESD Protection
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- This is a Pb−Free and Halogen−Free Device

Mechanical Characteristics:
CASE: Void-free, transfer-molded, thermosetting plastic Epoxy Meets UL 94 V−0
LEAD FINISH: 100% Matte Sn (Tin)
MOUNTING POSITION: Any
QUALIFIED MAX REFLOW TEMPERATURE: 260°C
Device Meets MSL 1 Requirements

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
IEC 61000−4−2 (ESD)	Contact Air		±10 ±15	kV
HBM			±16	
Total Power Dissipation on FR−5 Board (Note 1) @ T_A = 25°C		P_D	150	mW
Storage Temperature Range		T_{stg}	−55 to +150	°C
Junction Temperature Range		T_J	−55 to +125	°C
Lead Solder Temperature − Maximum (10 Second Duration)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. I_F, FR−5 = 1.0 x 0.75 x 0.62 in.
See Application Note AND8308/D for further description of survivability specs.

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SOD−923
CASE 514AB

MARKING DIAGRAM

J = Specific Device Code
M = Date Code
*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
ESD9R3.3ST5G	SOD−923 (Pb−Free)	8000 / Tape & Reel
SZESD9R3.3ST5G	SOD−923 (Pb−Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DEVICE MARKING INFORMATION

See specific marking information in the device marking column of the Electrical Characteristics tables starting on page 2 of this data sheet.

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