

Structured Electronic Design

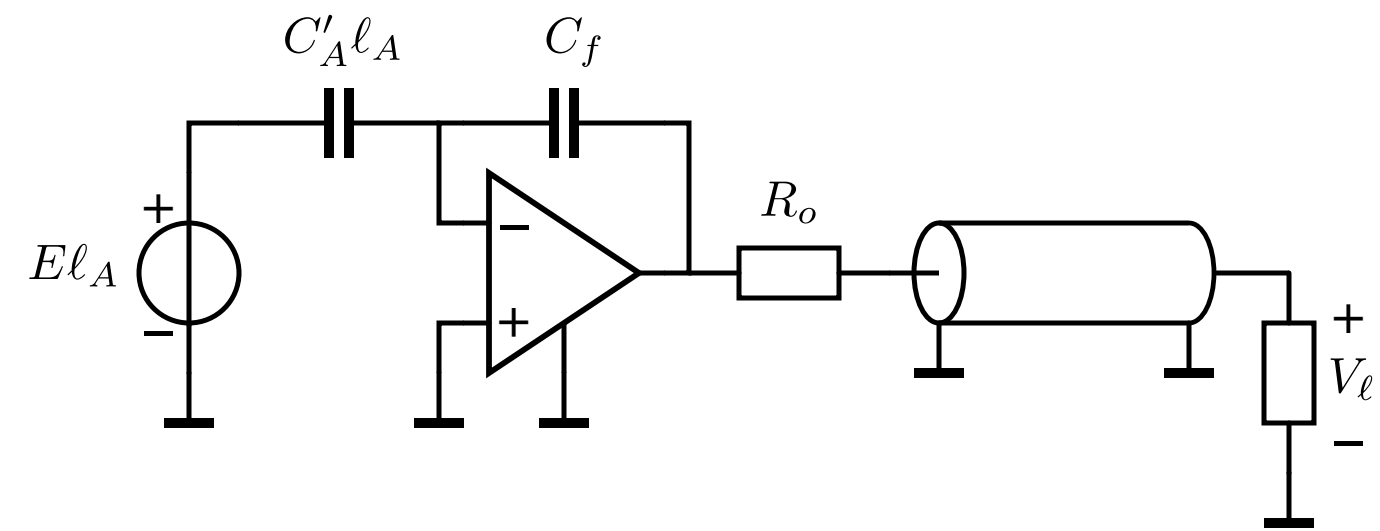
EE4109

Active antenna
Controller design

Anton J.M. Montagne

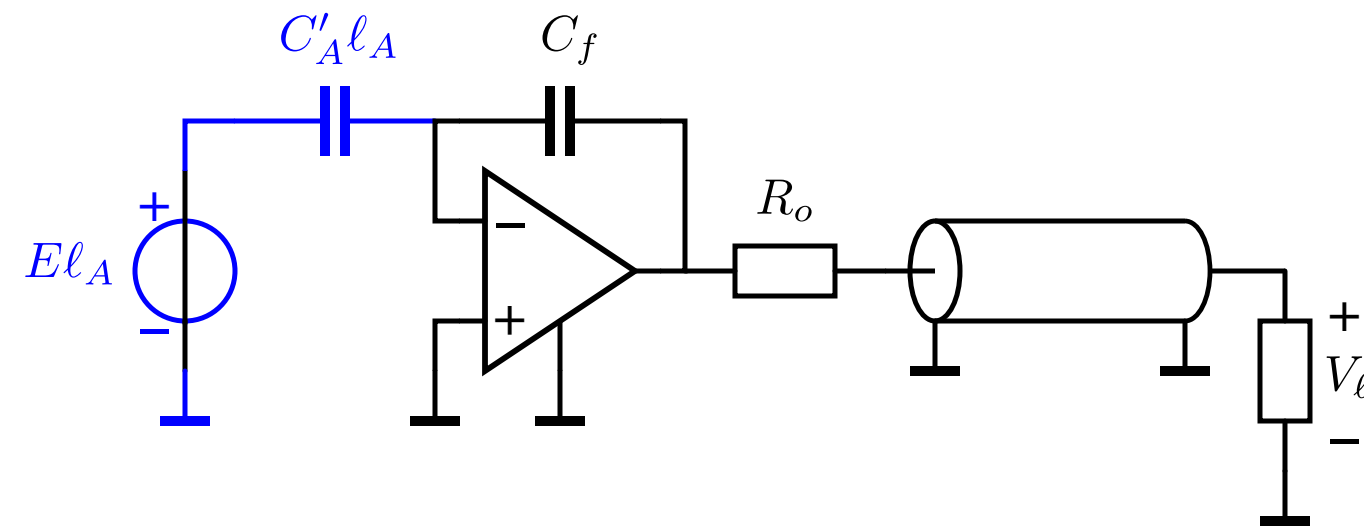
Active antenna

Active antenna



Active antenna

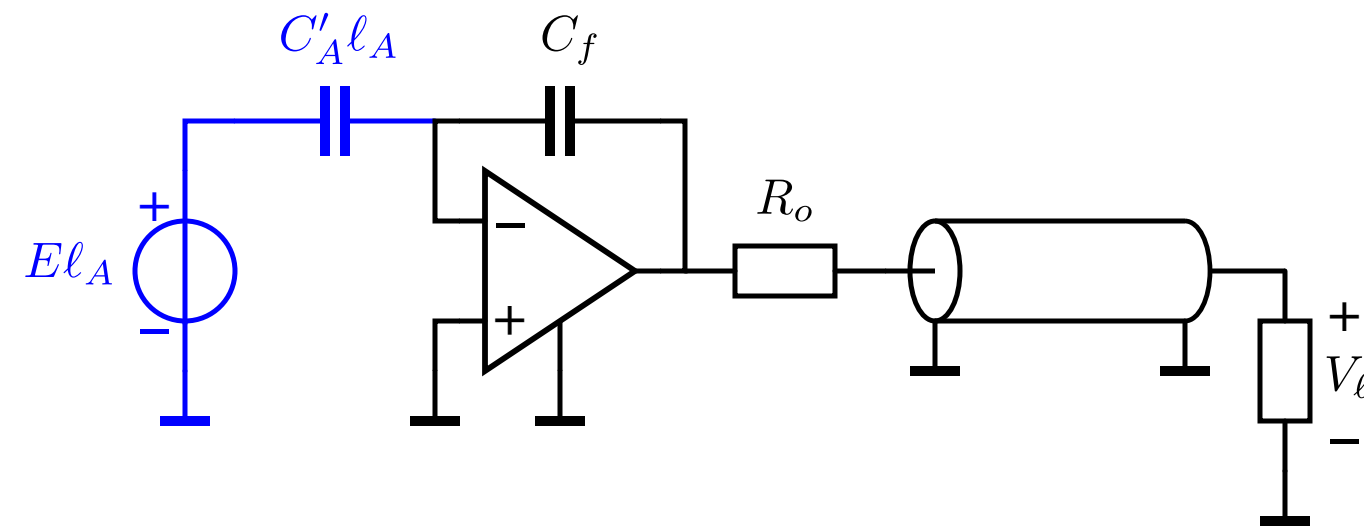
Antenna



Active antenna

Antenna

E-field to voltage conversion

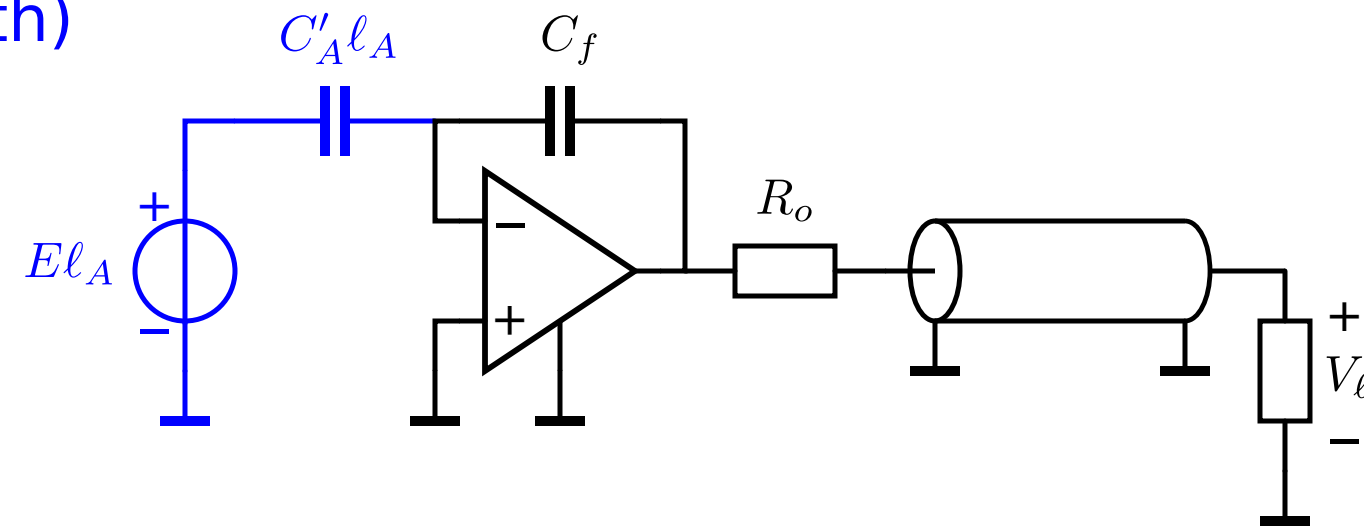


Active antenna

Antenna

E-field to voltage
conversion

Gain
(length)

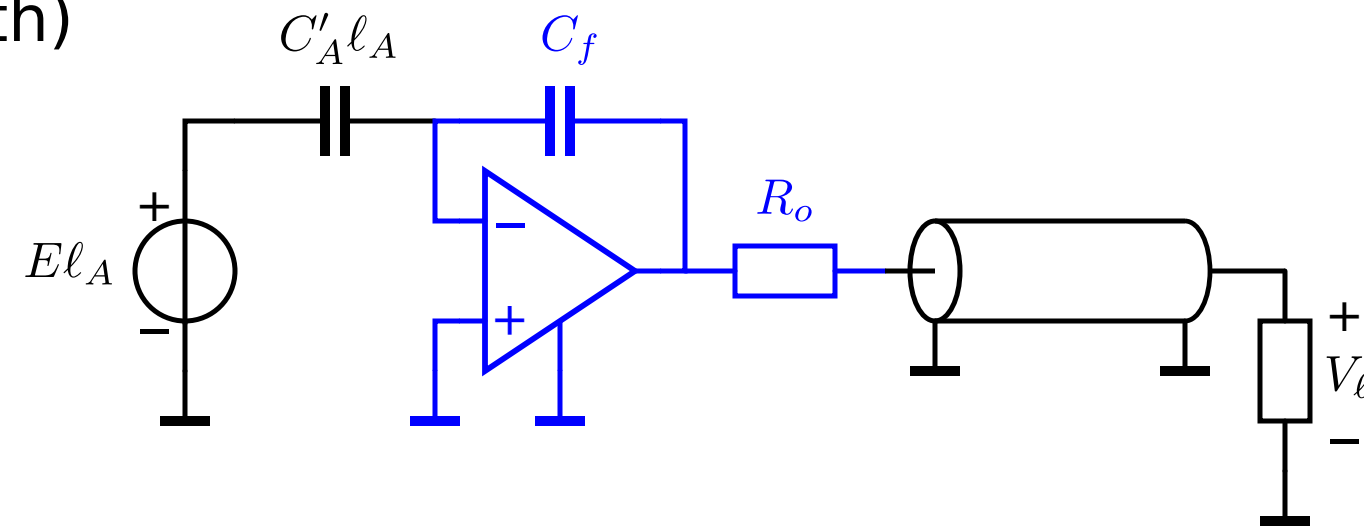


Active antenna

Antenna

E-field to voltage
conversion

Gain
(length)



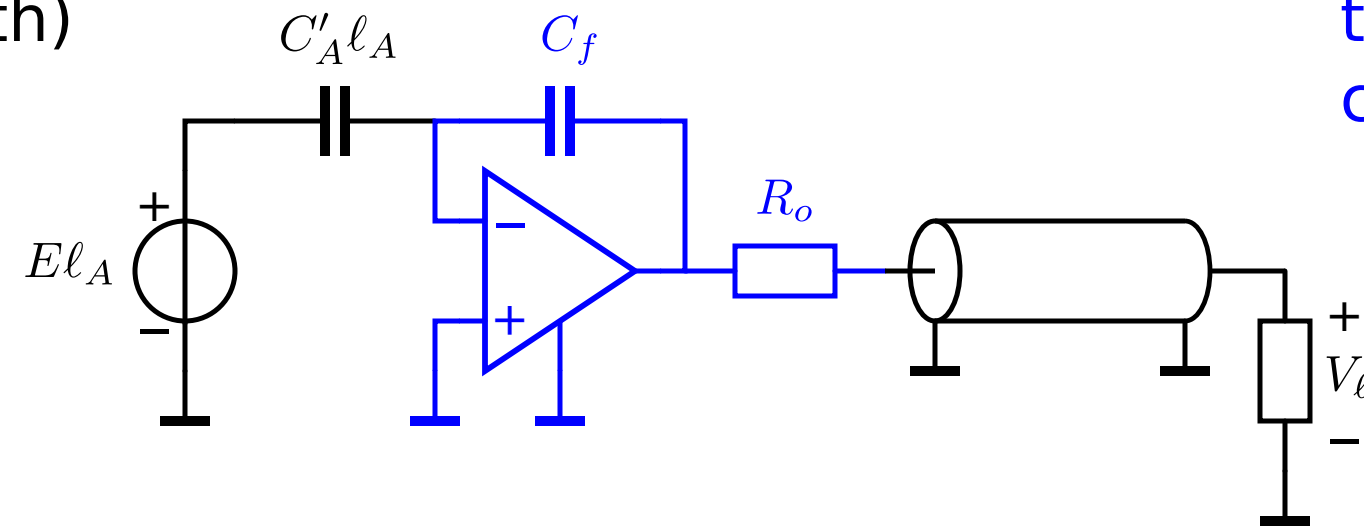
Amplifier

Active antenna

Antenna

E-field to voltage conversion

Gain (length)



Amplifier

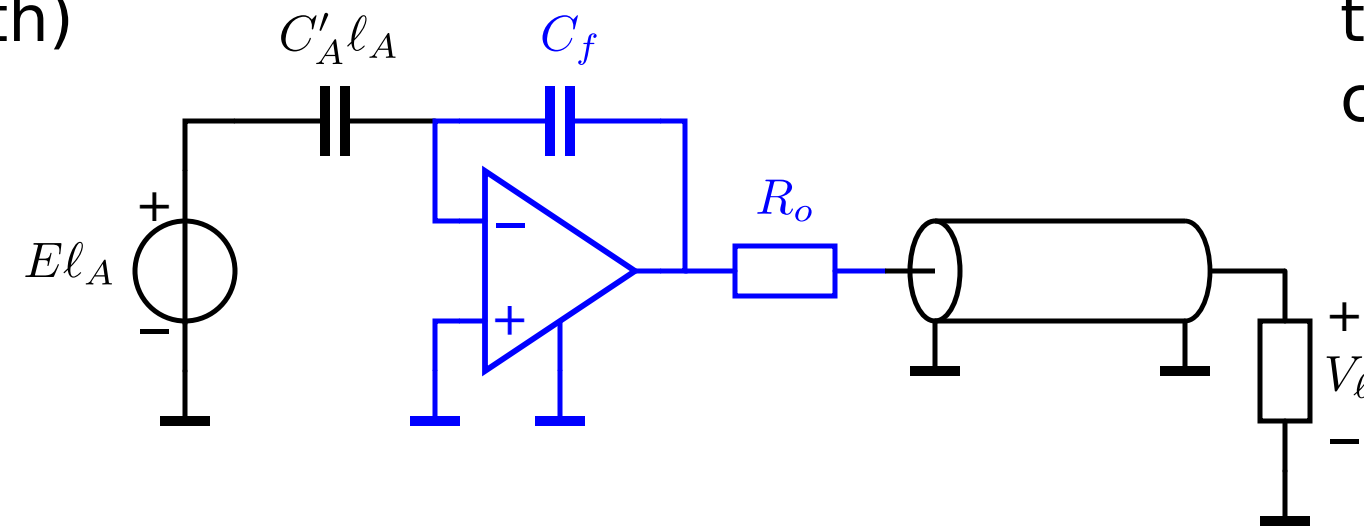
Integrating transimpedance cable driver

Active antenna

Antenna

E-field to voltage conversion

Gain (length)



Amplifier

Integrating transimpedance cable driver

Gain and output resistance

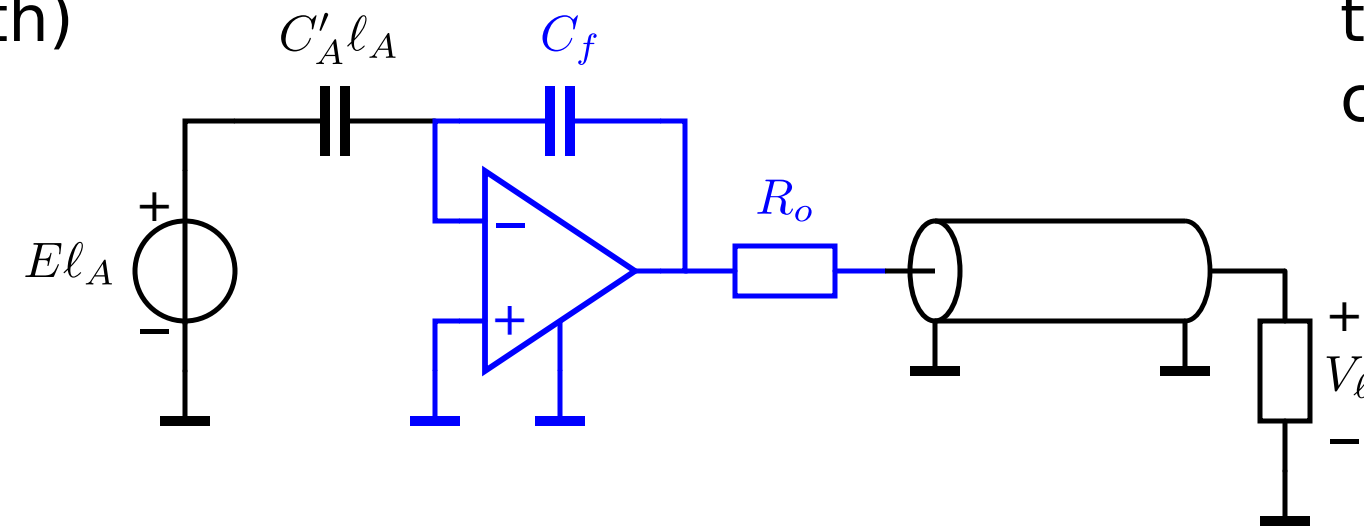
Active antenna

Antenna

E-field to voltage conversion
Gain (length)

Amplifier

Integrating transimpedance cable driver
Gain and output resistance
Noise



Feedback network

Capacitor
Capacitance
Accuracy

Controller or error amplifier

Single-stage or multi-stage amplifier
Equivalent-input noise sources
VI-drive capability
Midband loop gain
Loop gain-poles product
Differential error to loop gain ratio

Output resistor

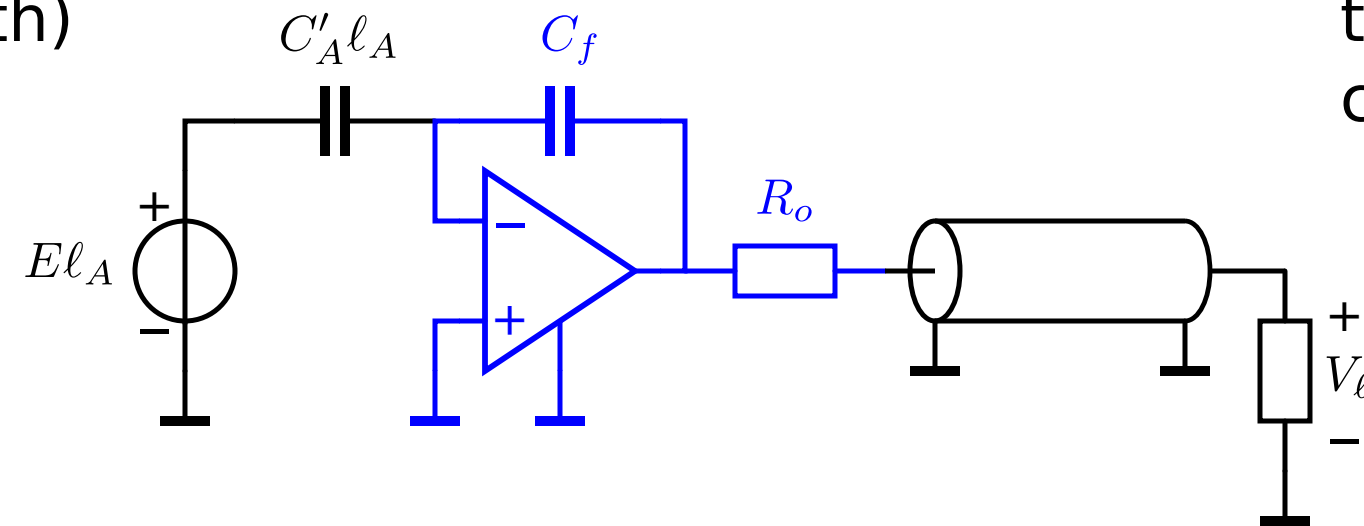
Resistor
Resistance
Accuracy

Active antenna

Antenna

E-field to voltage conversion

Gain (length)



Amplifier

Integrating transimpedance cable driver

Gain and output resistance

Noise

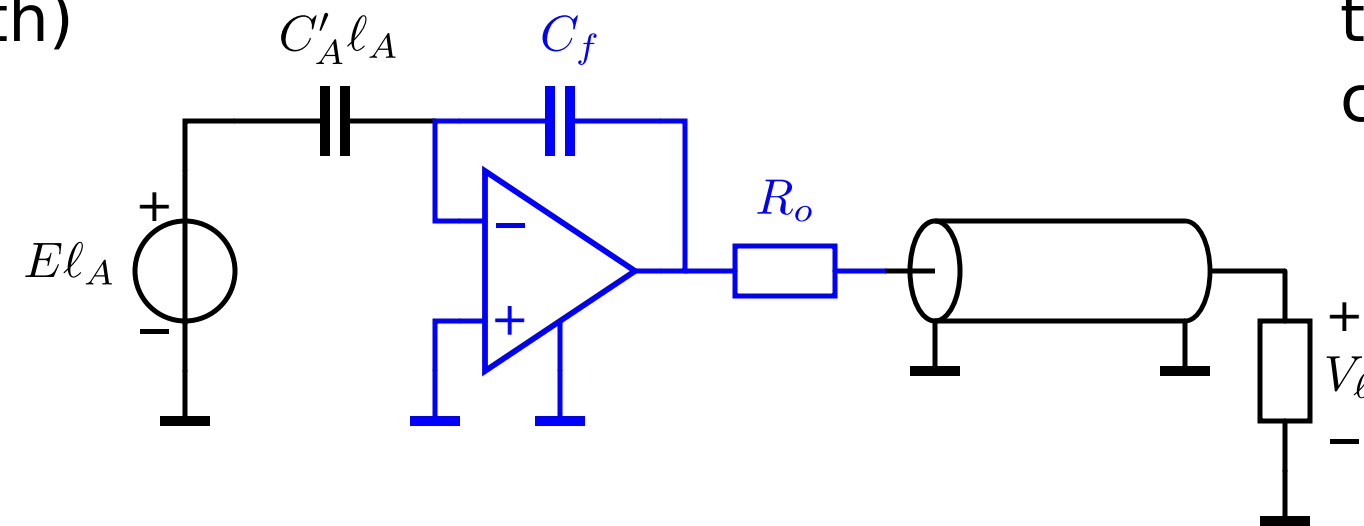
VI-drive capability

Active antenna

Antenna

E-field to voltage conversion

Gain (length)



Amplifier

Integrating transimpedance cable driver

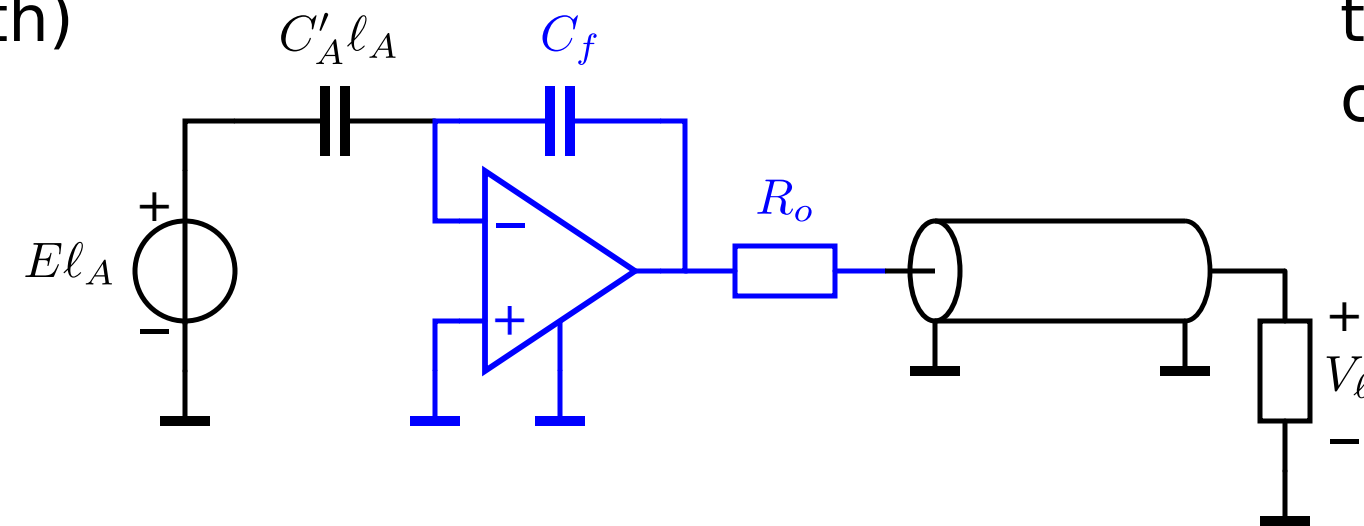
Gain and output resistance
Noise
VI-drive capability
Midband accuracy

Active antenna

Antenna

E-field to voltage conversion

Gain (length)



Amplifier

Integrating transimpedance cable driver

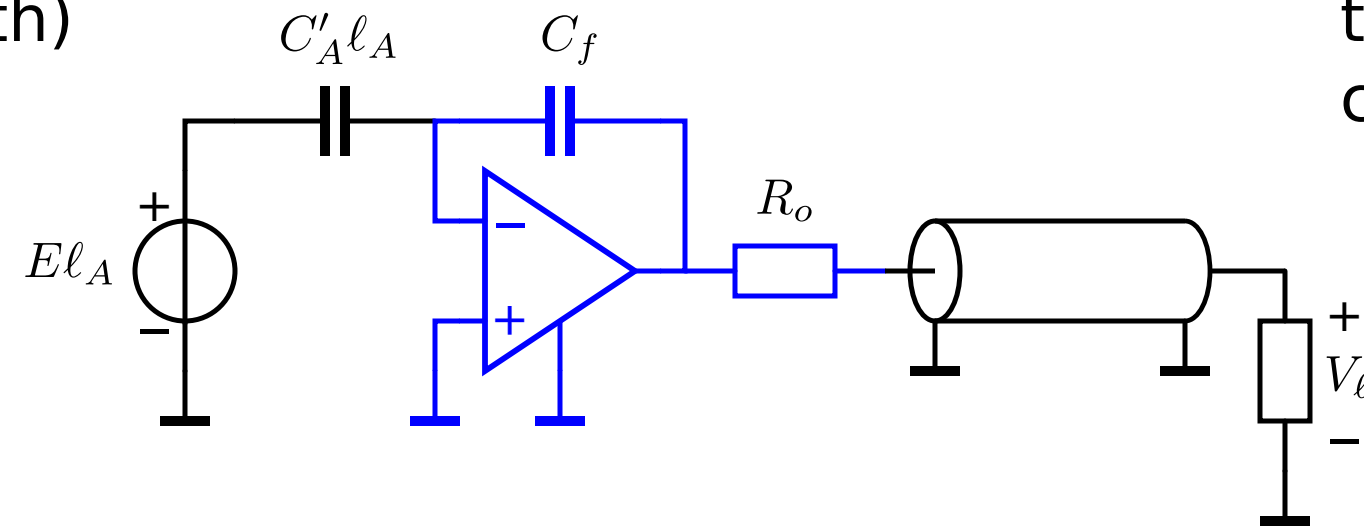
Gain and output resistance
Noise
VI-drive capability
Midband accuracy
Bandwidth

Active antenna

Antenna

E-field to voltage conversion

Gain (length)



Amplifier

Integrating transimpedance cable driver

Gain and output resistance

Noise

VI-drive capability

Midband accuracy

Bandwidth

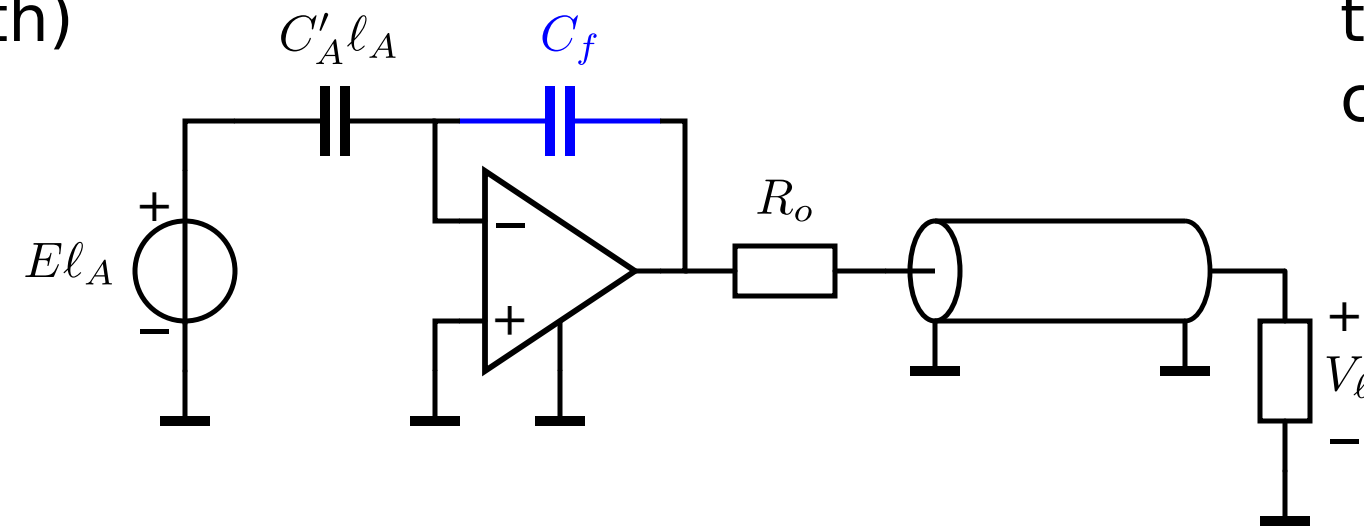
Weak nonlinearity

Active antenna

Antenna

E-field to voltage conversion

Gain (length)



Amplifier

Integrating transimpedance cable driver

Gain and output resistance

Noise

VI-drive capability

Midband accuracy

Bandwidth

Weak nonlinearity

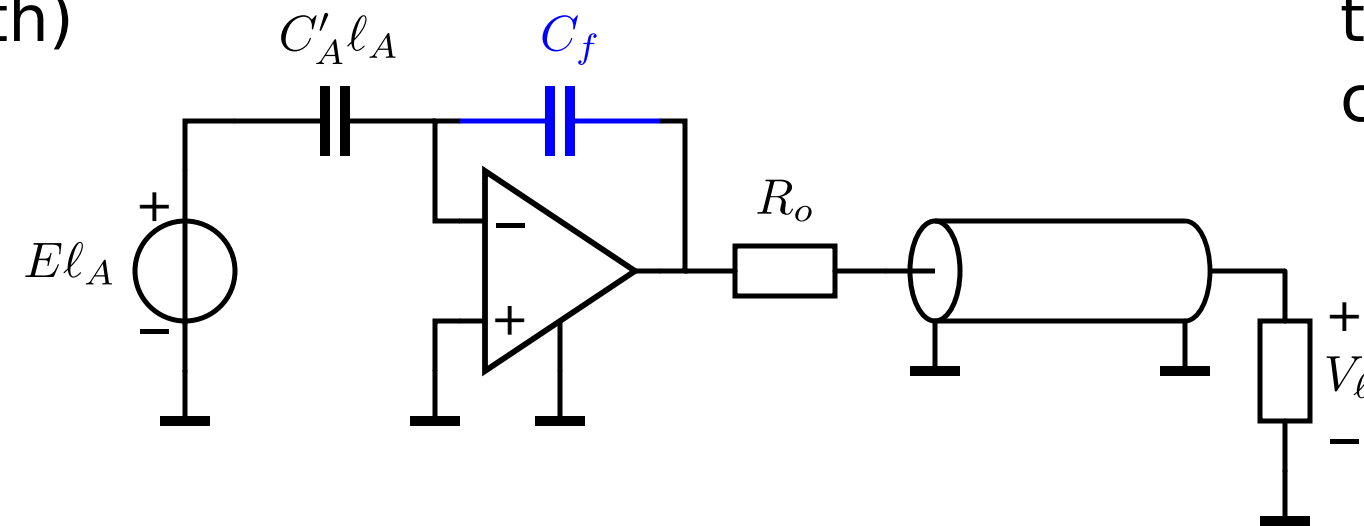
Feedback network

Active antenna

Antenna

E-field to voltage conversion

Gain (length)



Amplifier

Integrating transimpedance cable driver

Gain and output resistance

Noise

VI-drive capability

Midband accuracy

Bandwidth

Weak nonlinearity

Feedback network

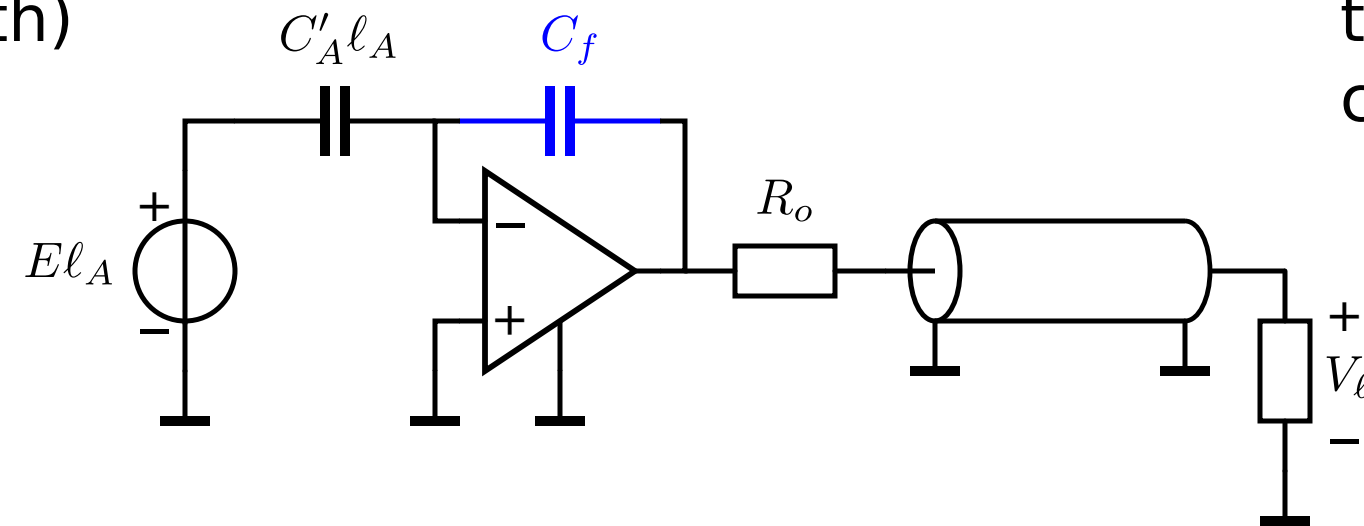
Capacitor

Active antenna

Antenna

E-field to voltage conversion

Gain (length)



Amplifier

Integrating transimpedance cable driver

Gain and output resistance

Noise

VI-drive capability

Midband accuracy

Bandwidth

Weak nonlinearity

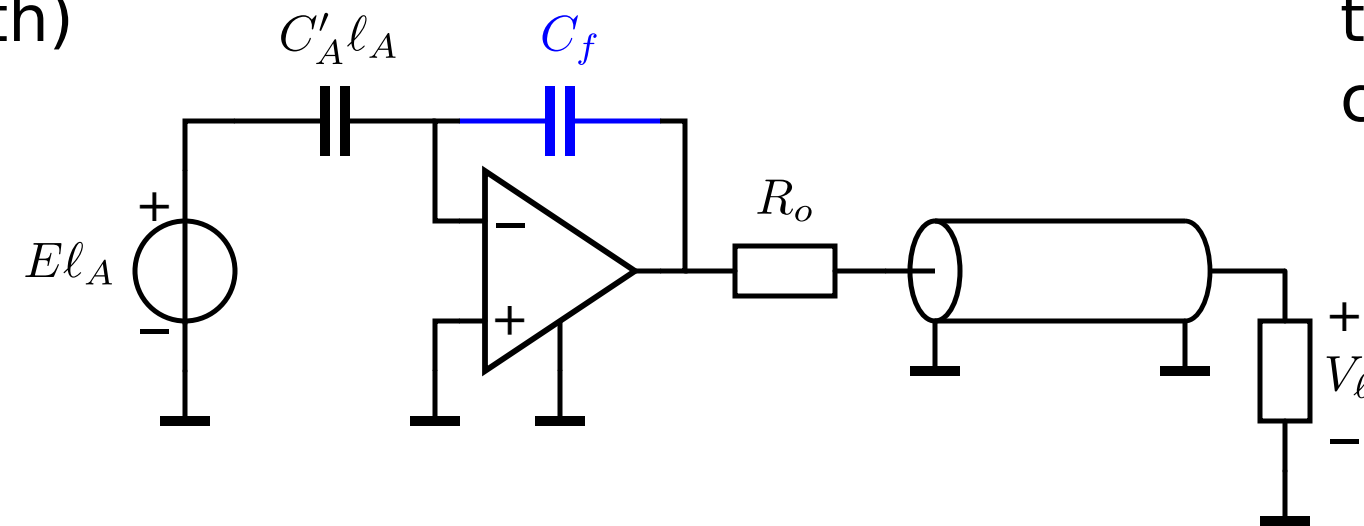
Feedback network

Capacitor Capacitance

Active antenna

Antenna

E-field to voltage conversion
Gain (length)



Amplifier

Integrating transimpedance cable driver
Gain and output resistance
Noise
VI-drive capability
Midband accuracy
Bandwidth
Weak nonlinearity

Feedback network

Capacitor Capacitance
Accuracy

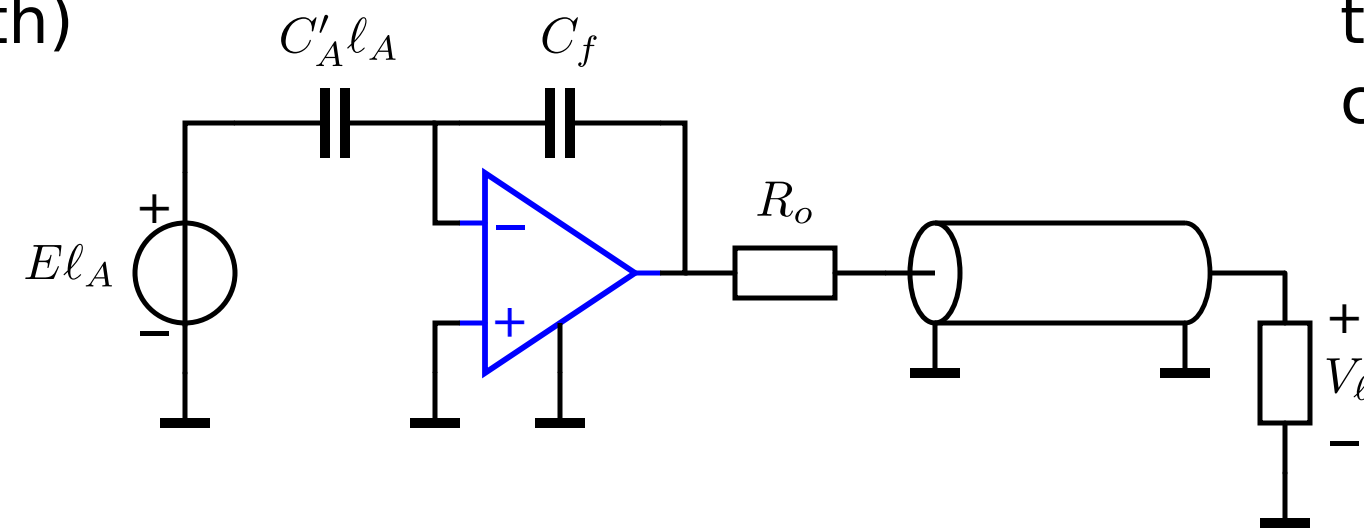
Active antenna

Antenna

E-field to voltage conversion
Gain (length)

Amplifier

Integrating transimpedance cable driver
Gain and output resistance
Noise
VI-drive capability
Midband accuracy
Bandwidth
Weak nonlinearity



Feedback network

Capacitor Capacitance
Accuracy

Controller or error amplifier

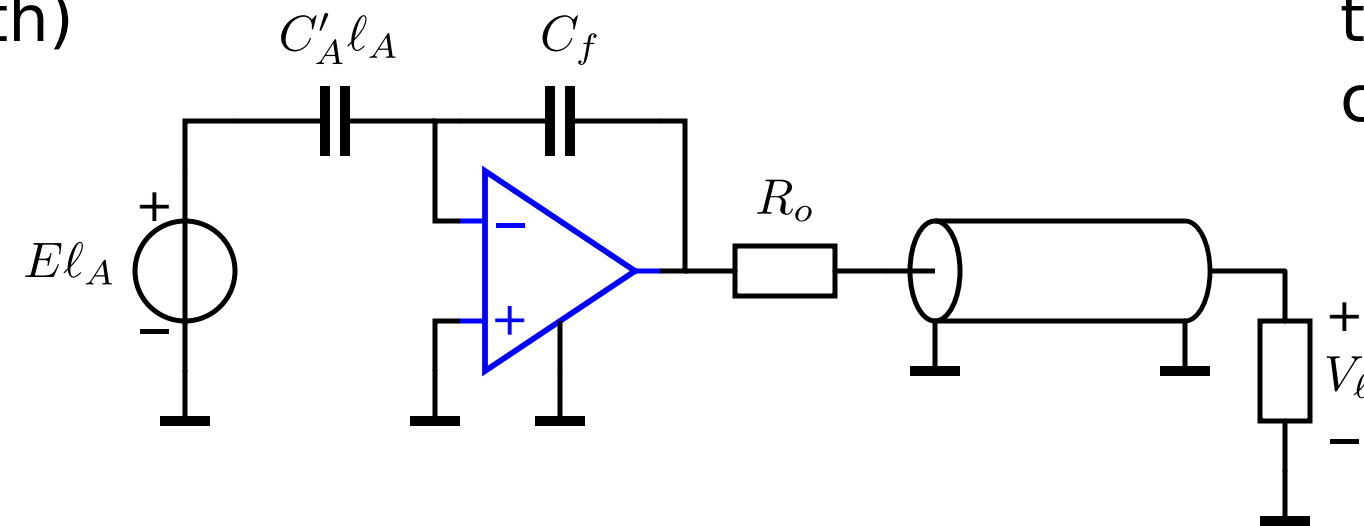
Active antenna

Antenna

E-field to voltage conversion
Gain (length)

Amplifier

Integrating transimpedance cable driver
Gain and output resistance
Noise
VI-drive capability
Midband accuracy
Bandwidth
Weak nonlinearity



Feedback network

Capacitor Capacitance
Accuracy

Controller or error amplifier

Single-stage or multi-stage amplifier

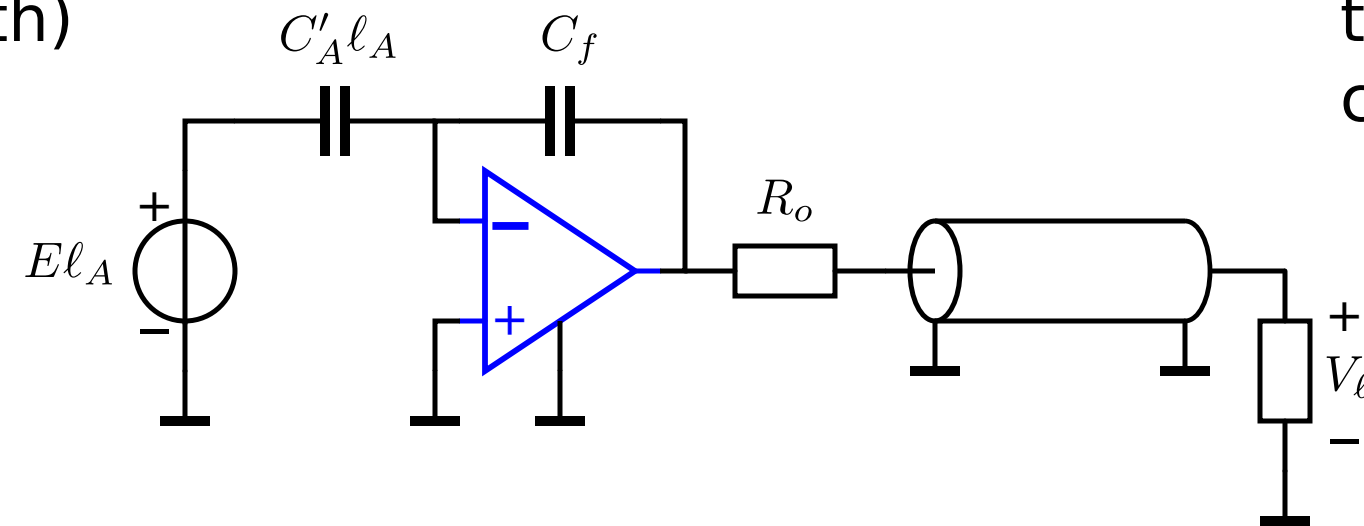
Active antenna

Antenna

E-field to voltage conversion
Gain (length)

Amplifier

Integrating transimpedance cable driver
Gain and output resistance
Noise
VI-drive capability
Midband accuracy
Bandwidth
Weak nonlinearity



Feedback network

Capacitor
Capacitance
Accuracy

Controller or error amplifier

Single-stage or multi-stage amplifier
Equivalent-input noise sources

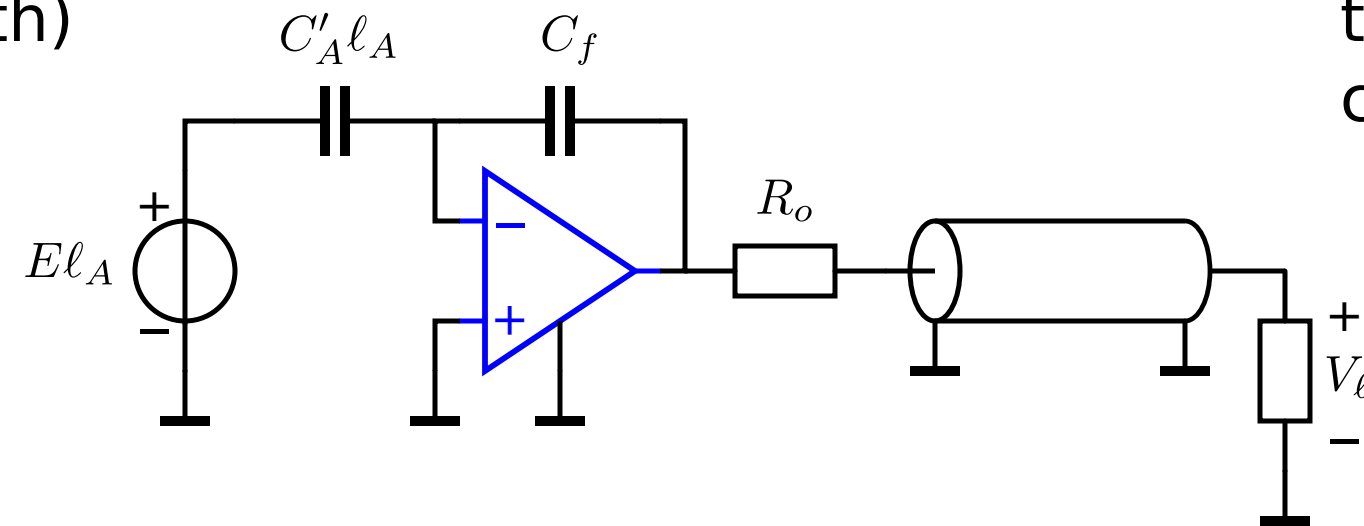
Active antenna

Antenna

E-field to voltage conversion
Gain (length)

Amplifier

Integrating transimpedance cable driver
Gain and output resistance
Noise
VI-drive capability
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Feedback network

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Capacitance
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Controller or error amplifier

Single-stage or multi-stage amplifier
Equivalent-input noise sources
VI-drive capability

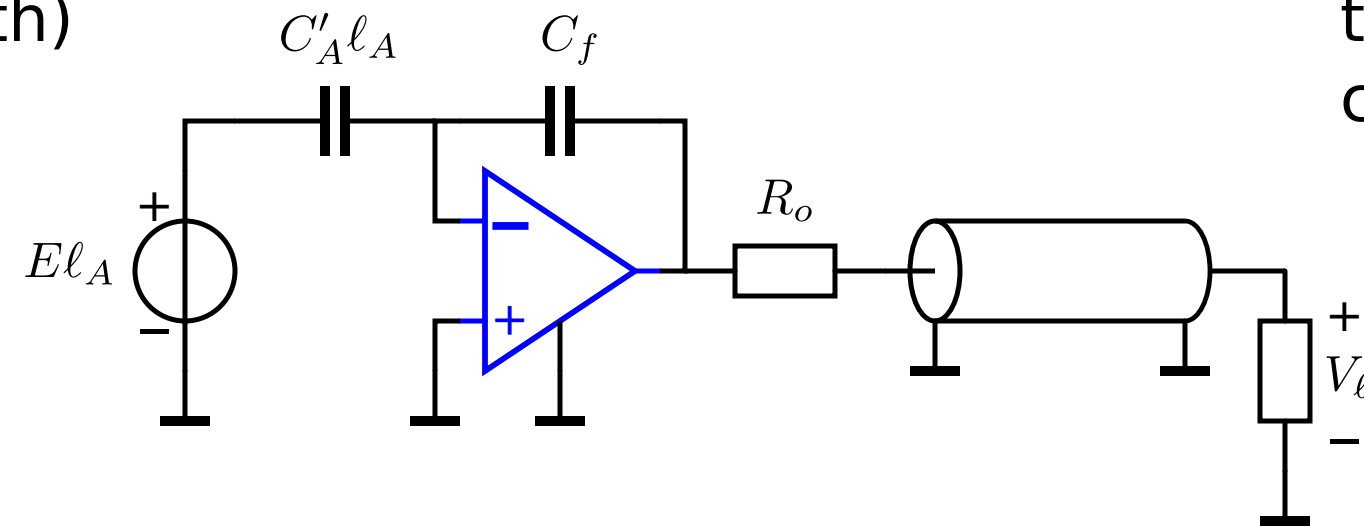
Active antenna

Antenna

E-field to voltage conversion
Gain (length)

Amplifier

Integrating transimpedance cable driver
Gain and output resistance
Noise
VI-drive capability
Midband accuracy
Bandwidth
Weak nonlinearity



Feedback network

Capacitor
Capacitance
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Controller or error amplifier

Single-stage or multi-stage amplifier
Equivalent-input noise sources
VI-drive capability
Midband loop gain (contribution)

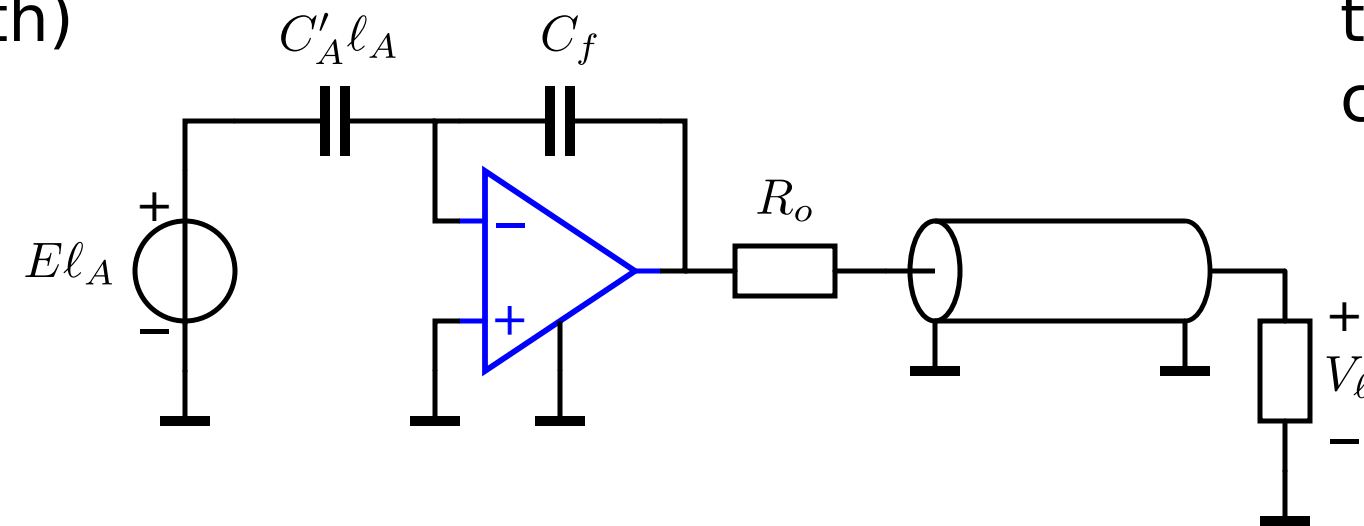
Active antenna

Antenna

E-field to voltage conversion
Gain (length)

Amplifier

Integrating transimpedance cable driver
Gain and output resistance
Noise
VI-drive capability
Midband accuracy
Bandwidth
Weak nonlinearity



Feedback network

Capacitor
Capacitance
Accuracy

Controller or error amplifier

Single-stage or multi-stage amplifier
Equivalent-input noise sources
VI-drive capability
Midband loop gain (contribution)
Loop gain-poles product (contribution)

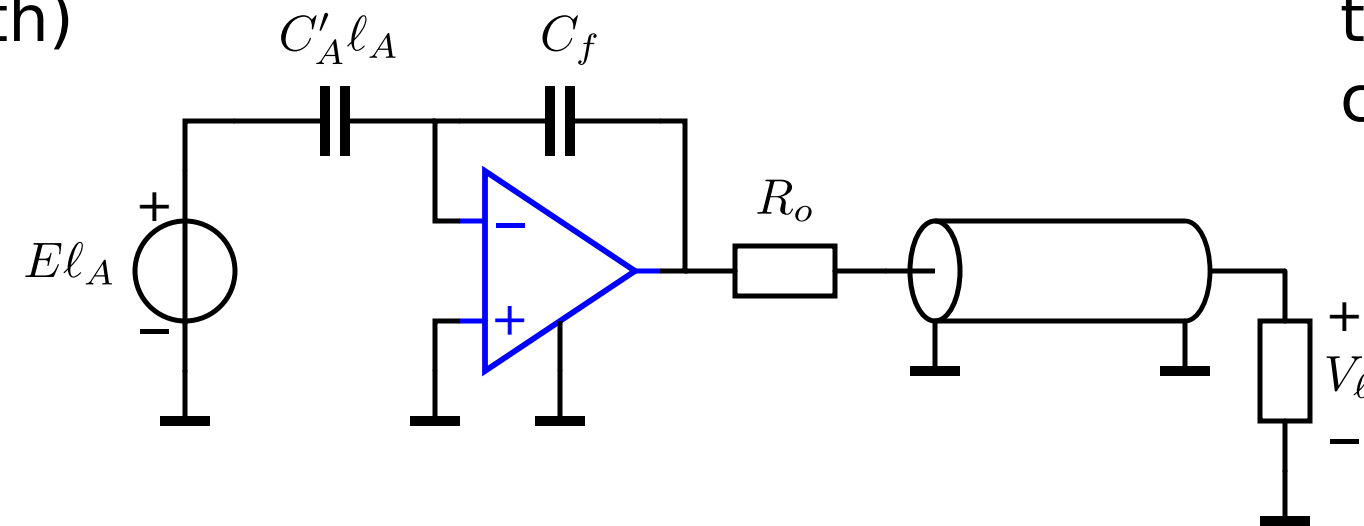
Active antenna

Antenna

E-field to voltage conversion
Gain (length)

Amplifier

Integrating transimpedance cable driver
Gain and output resistance
Noise
VI-drive capability
Midband accuracy
Bandwidth
Weak nonlinearity



Feedback network

Capacitor
Capacitance
Accuracy

Controller or error amplifier

Single-stage or multi-stage amplifier
Equivalent-input noise sources
VI-drive capability
Midband loop gain (contribution)
Loop gain-poles product (contribution)
Differential error to loop gain ratio (contribution)

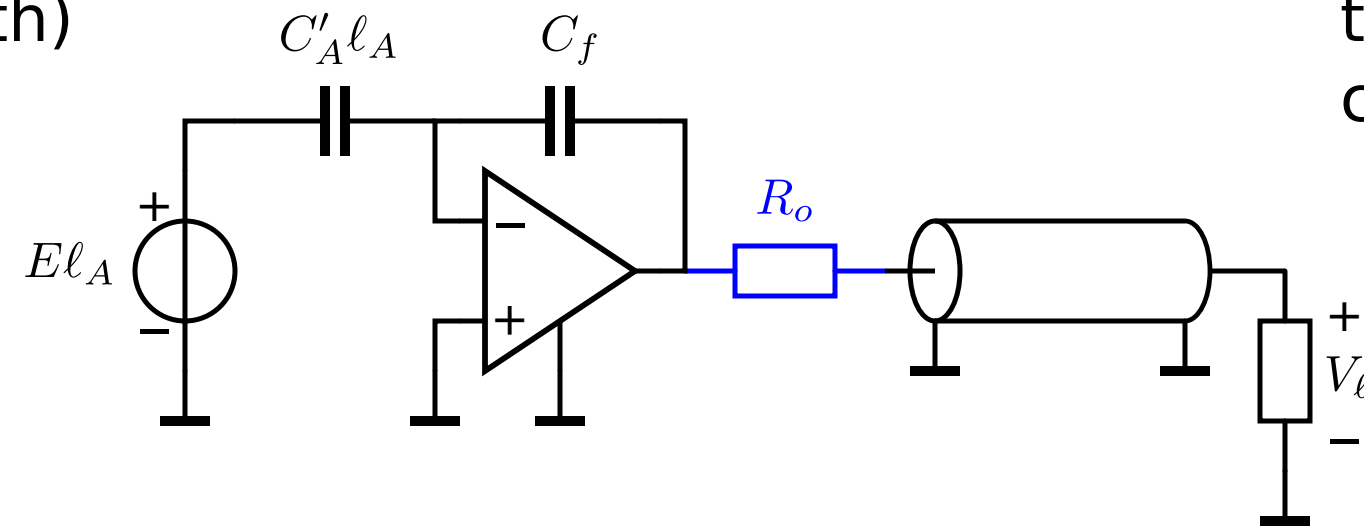
Active antenna

Antenna

E-field to voltage conversion
Gain (length)

Amplifier

Integrating transimpedance cable driver
Gain and output resistance
Noise
VI-drive capability
Midband accuracy
Bandwidth
Weak nonlinearity



Feedback network

Capacitor
Capacitance
Accuracy

Controller or error amplifier

Single-stage or multi-stage amplifier
Equivalent-input noise sources
VI-drive capability
Midband loop gain (contribution)
Loop gain-poles product (contribution)
Differential error to loop gain ratio (contribution)

Output resistor

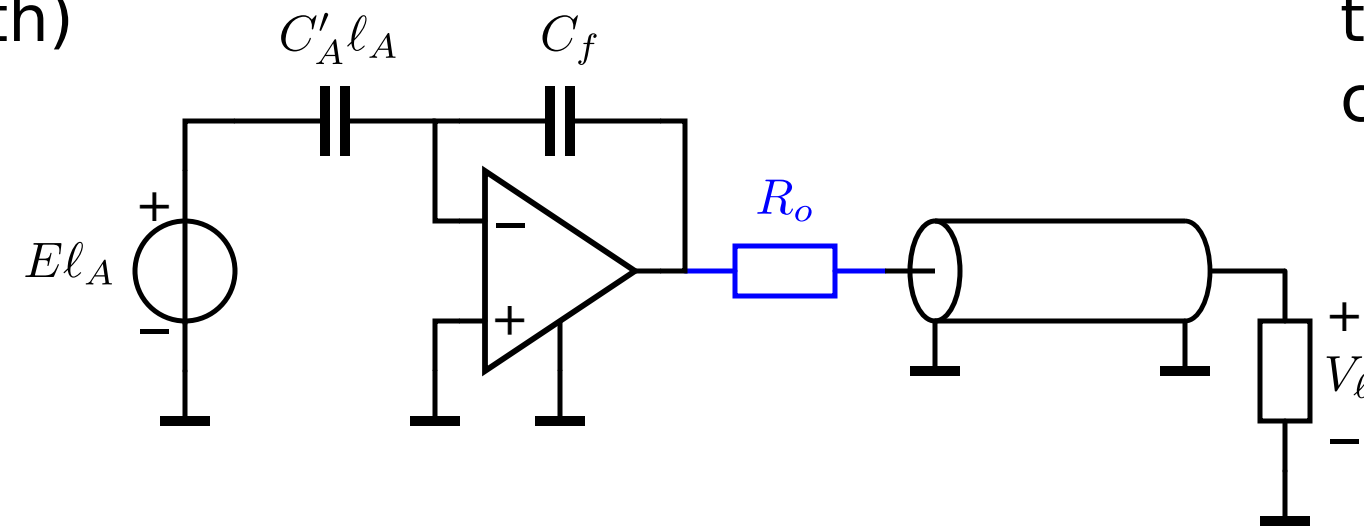
Active antenna

Antenna

E-field to voltage conversion
Gain (length)

Amplifier

Integrating transimpedance cable driver
Gain and output resistance
Noise
VI-drive capability
Midband accuracy
Bandwidth
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Feedback network

Capacitor
Capacitance
Accuracy

Controller or error amplifier

Single-stage or multi-stage amplifier
Equivalent-input noise sources
VI-drive capability
Midband loop gain (contribution)
Loop gain-poles product (contribution)
Differential error to loop gain ratio (contribution)

Output resistor

Resistor

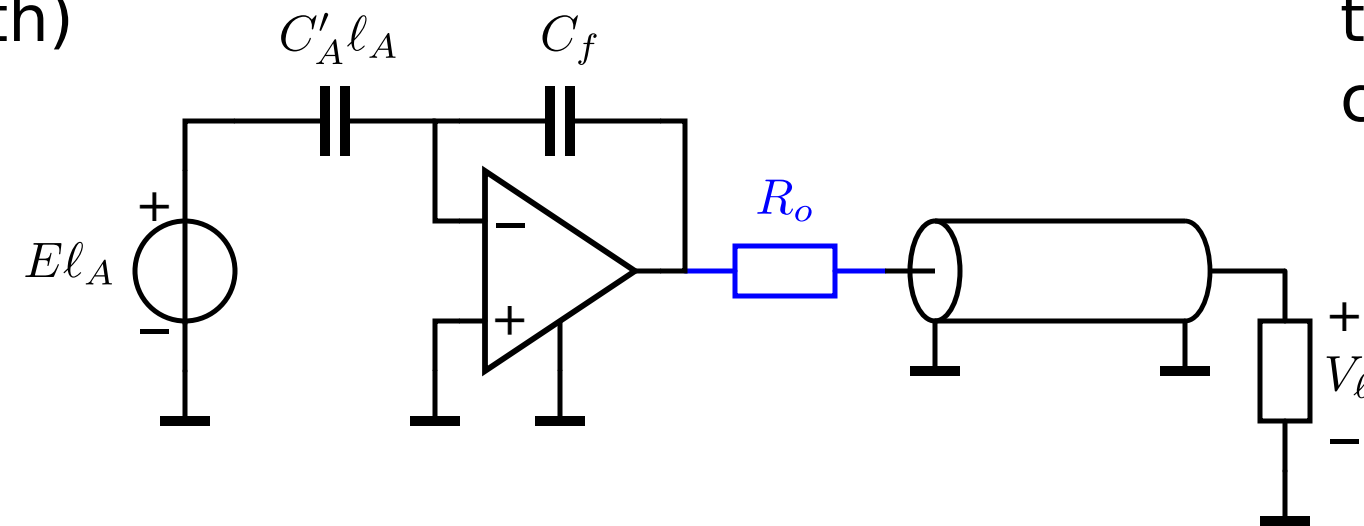
Active antenna

Antenna

E-field to voltage conversion
Gain (length)

Amplifier

Integrating transimpedance cable driver
Gain and output resistance
Noise
VI-drive capability
Midband accuracy
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Feedback network

Capacitor
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Controller or error amplifier

Single-stage or multi-stage amplifier
Equivalent-input noise sources
VI-drive capability
Midband loop gain (contribution)
Loop gain-poles product (contribution)
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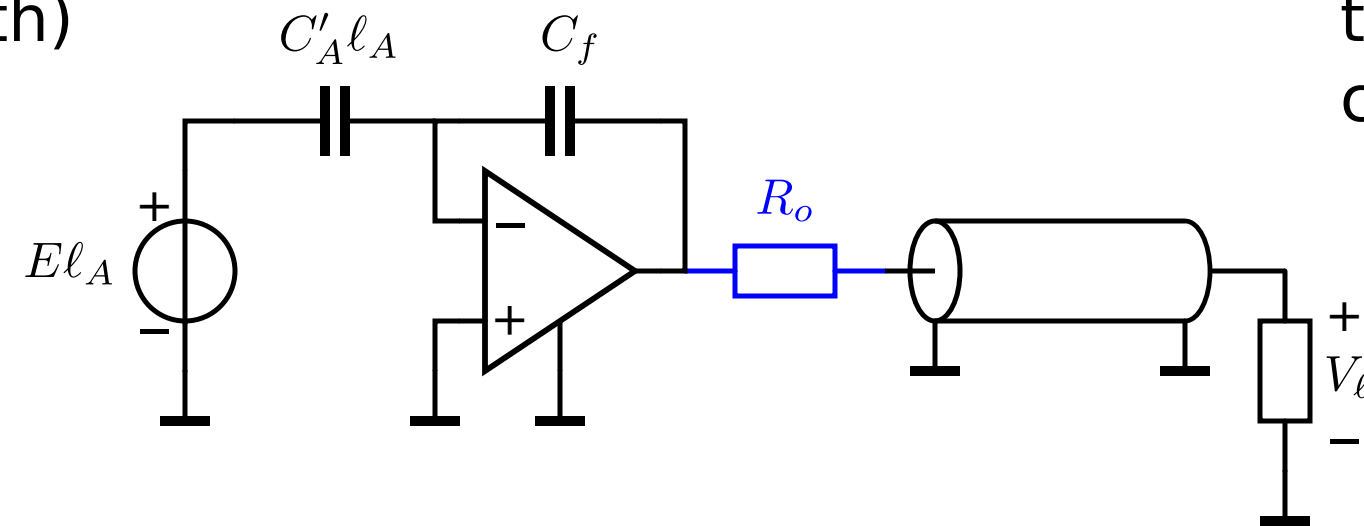
Output resistor

Resistor **Resistance**

Active antenna

Antenna

E-field to voltage conversion
Gain (length)



Amplifier

Integrating transimpedance cable driver
Gain and output resistance
Noise
VI-drive capability
Midband accuracy
Bandwidth
Weak nonlinearity

Feedback network

Capacitor
Capacitance
Accuracy

Controller or error amplifier

Single-stage or multi-stage amplifier
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Midband loop gain (contribution)
Loop gain-poles product (contribution)
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Output resistor

Resistor
Resistance
Accuracy

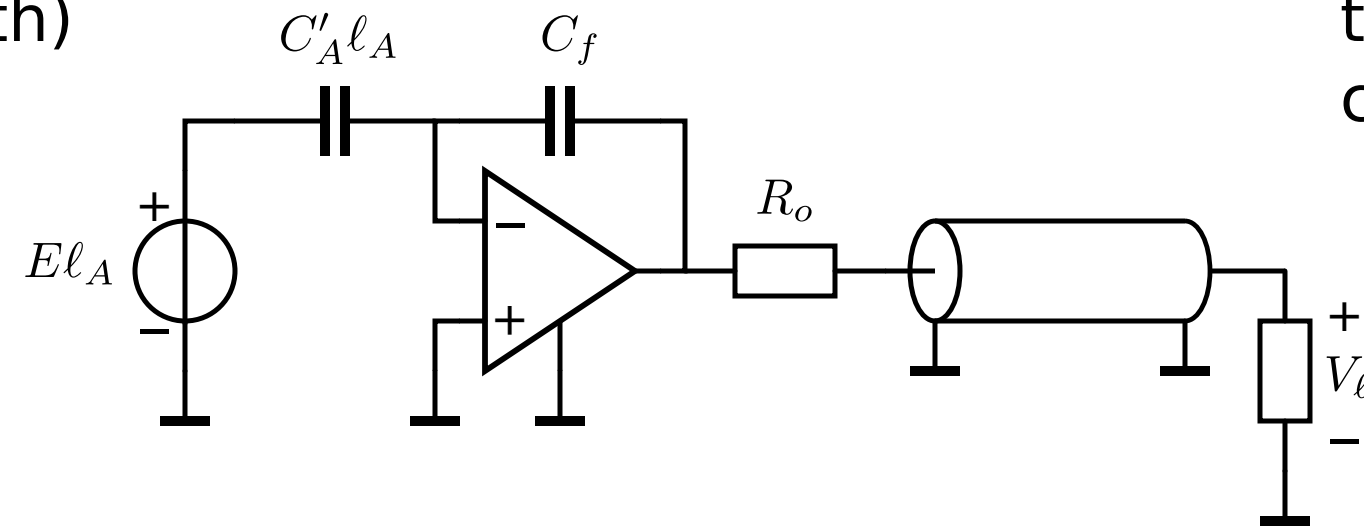
Active antenna

Antenna

E-field to voltage conversion
Gain (length)

Amplifier

Integrating transimpedance cable driver
Gain and output resistance
Noise
VI-drive capability
Midband accuracy
Bandwidth
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Feedback network

Capacitor
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Midband loop gain (contribution)
Loop gain-poles product (contribution)
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Output resistor

Resistor
Resistance
Accuracy

Structured Electronic Design

EE4109

Controller design:
Design considerations

Anton J.M. Montagne

Controller design

Controller design

Input stage:

Controller design

Input stage: Performance aspect: noise

Controller design

Input stage: Performance aspect: noise
Stage type: CS or balanced

Controller design

Input stage: Performance aspect: noise
Stage type: CS or balanced
Best nullor like stage: minimizes noise contributions of other stages

Controller design

Input stage: Performance aspect: noise
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Determine design limits for W , L and I_{DS}

Controller design

Input stage: Performance aspect: noise
Stage type: CS or balanced
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Determine design limits for W , L and I_{DS}

Output stage:

Controller design

- Input stage: Performance aspect: noise
Stage type: CS or balanced
Best nullor like stage: minimizes noise contributions of other stages
Determine design limits for W , L and I_{DS}
- Output stage: Performance aspects: VI-drive capability and power efficiency

Controller design

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Controller design

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Use smallest $L_{P,N}$, and determine design limits for $W_{P,N}$, $V_{DSP,N}$ and I_Q

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Single-stage

Controller design

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Single-stage

Noise and VI-drive can be met with single stage

Controller design

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Single-stage

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Dual-stage

Controller design

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Single-stage

Noise and VI-drive can be met with single stage

Dual-stage

Noise performance can be met

Controller design

- Input stage:** Performance aspect: noise
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Single-stage

Noise and VI-drive can be met with single stage

Dual-stage

Noise performance can be met
1-st stage can drive 2-nd stage

Controller design

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Single-stage

Noise and VI-drive can be met with single stage

Dual-stage

Noise performance can be met
1-st stage can drive 2-nd stage
2-nd stage can drive the load

Controller design

- Input stage:** Performance aspect: noise
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Single-stage

Noise and VI-drive can be met with single stage

Dual-stage

Noise performance can be met
1-st stage can drive 2-nd stage
2-nd stage can drive the load

Multiple-stage

Controller design

- Input stage:** Performance aspect: noise
Stage type: CS or balanced
Best nullor like stage: minimizes noise contributions of other stages
Determine design limits for W , L and I_{DS}
- Output stage:** Performance aspects: VI-drive capability and power efficiency
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Single-stage

Noise and VI-drive can be met with single stage

Dual-stage

Noise performance can be met
1-st stage can drive 2-nd stage
2-nd stage can drive the load

Multiple-stage

Noise performance can be met

Controller design

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Single-stage

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Dual-stage

Noise performance can be met
1-st stage can drive 2-nd stage
2-nd stage can drive the load

Multiple-stage

Noise performance can be met
i-1-th stage can drive i-th stage

Controller design

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Single-stage

Noise and VI-drive can be met with single stage

Dual-stage

Noise performance can be met
1-st stage can drive 2-nd stage
2-nd stage can drive the load

Multiple-stage

Noise performance can be met
i-1-th stage can drive i-th stage
Last stage can drive the load

Controller design

- Input stage:** Performance aspect: noise
Stage type: CS or balanced
Best nullor like stage: minimizes noise contributions of other stages
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Single-stage

Noise and VI-drive can be met with single stage

Dual-stage

Noise performance can be met
1-st stage can drive 2-nd stage
2-nd stage can drive the load

Multiple-stage

Noise performance can be met
 $i-1$ -th stage can drive i -th stage
Last stage can drive the load



Controller design

- Input stage:** Performance aspect: noise
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Single-stage

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Dual-stage

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1-st stage can drive 2-nd stage
2-nd stage can drive the load

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Noise performance can be met
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Last stage can drive the load



Midband loop gain is OK

Controller design

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Single-stage

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Dual-stage

Noise performance can be met
1-st stage can drive 2-nd stage
2-nd stage can drive the load

Multiple-stage

Noise performance can be met
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Last stage can drive the load



Midband loop gain is OK

Loop gain-poles product is OK

Controller design

- Input stage:** Performance aspect: noise
Stage type: CS or balanced
Best nullor like stage: minimizes noise contributions of other stages
Determine design limits for W , L and I_{DS}
- Output stage:** Performance aspects: VI-drive capability and power efficiency
Stage type: complementary parallel CS
Best nullor like stage: minimizes distortion contributions of other stages
Complementary parallel: improved power efficiency when operating in class AB mode
Use smallest $L_{P,N}$, and determine design limits for $W_{P,N}$, $V_{DSP,N}$ and I_Q

Single-stage

Noise and VI-drive can be met with single stage

Dual-stage

Noise performance can be met
1-st stage can drive 2-nd stage
2-nd stage can drive the load

Multiple-stage

Noise performance can be met
i-1-th stage can drive i-th stage
Last stage can drive the load



Midband loop gain is OK
Loop gain-poles product is OK
Diff. error to loop gain ratio is OK

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Loop gain-poles product

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? How much can a stage contribute to the product of the loop gain and the dominant poles

Loop gain-poles product

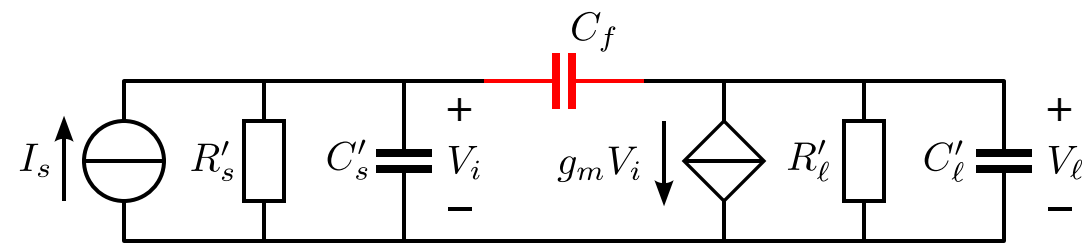
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Negative feedback in a stage:

Loop gain-poles product

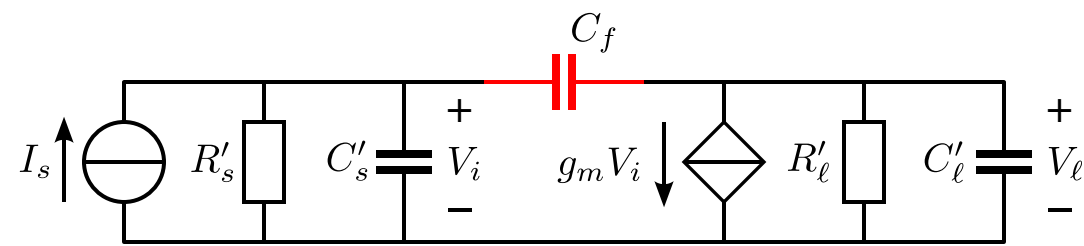
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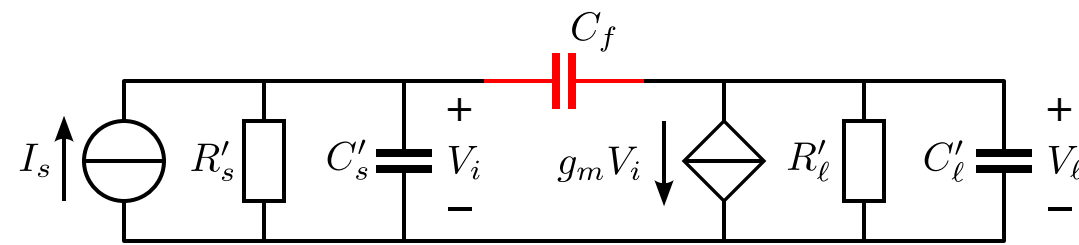


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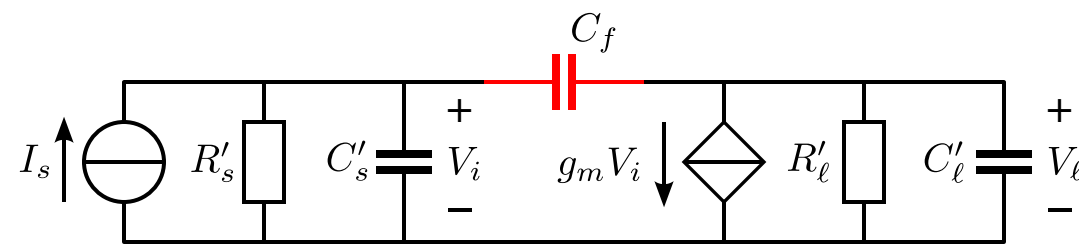
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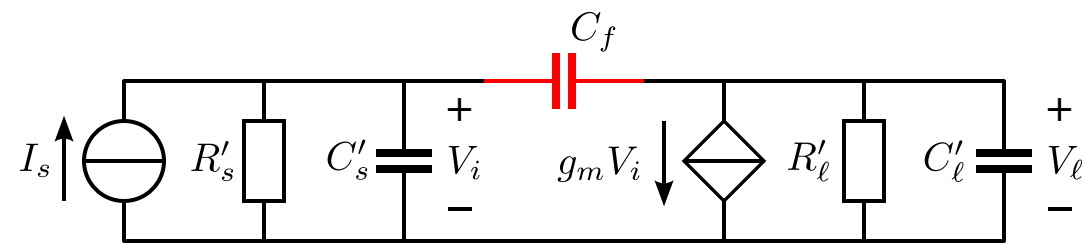
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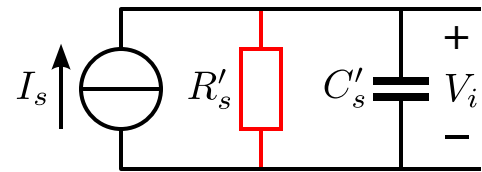


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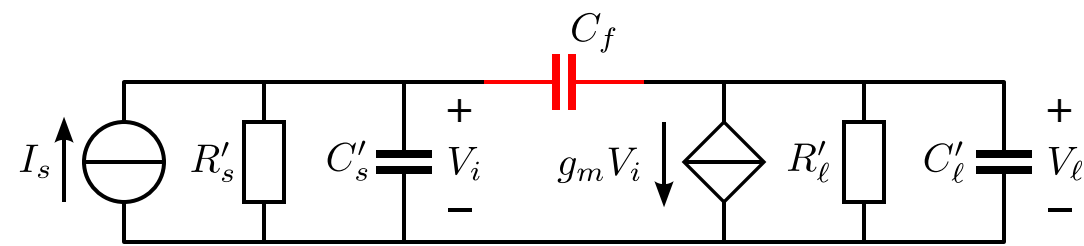
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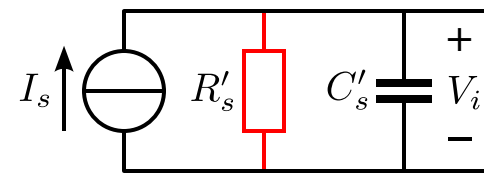
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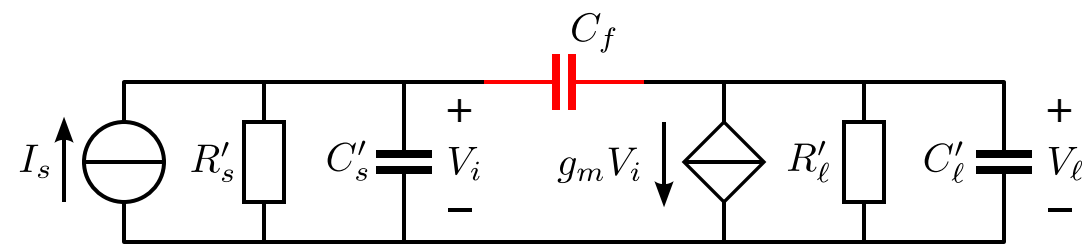


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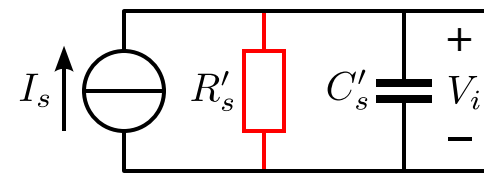
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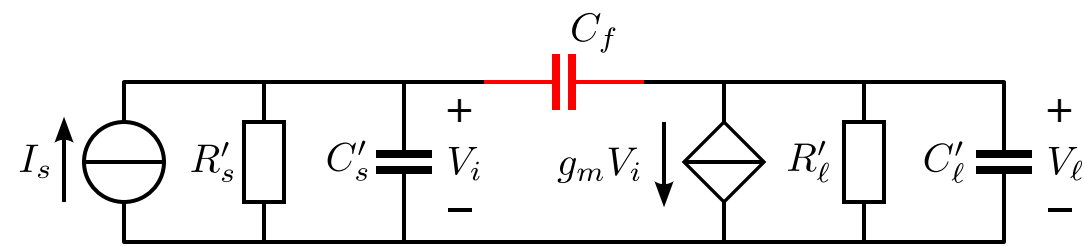


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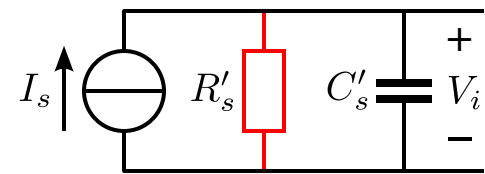
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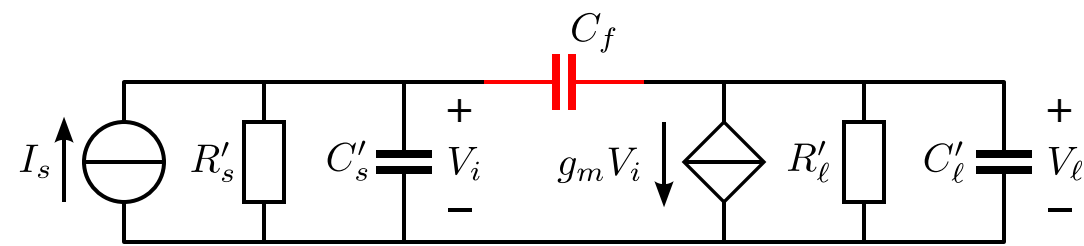
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Current-driven shorted CS stage (or balanced) has the largest contribution to the LP product

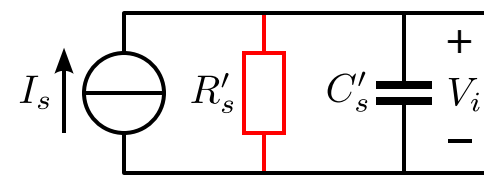
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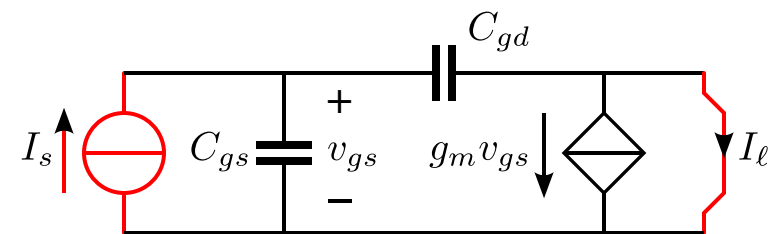
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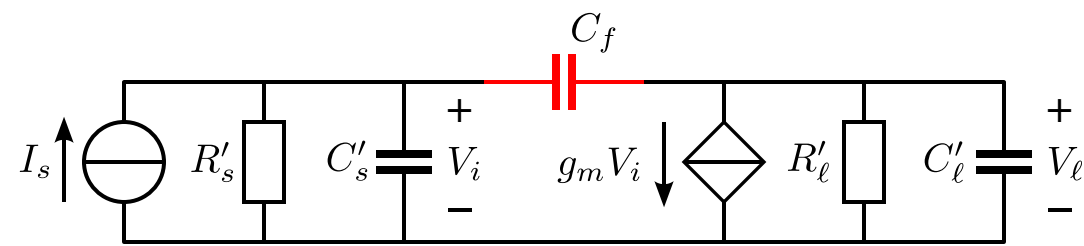
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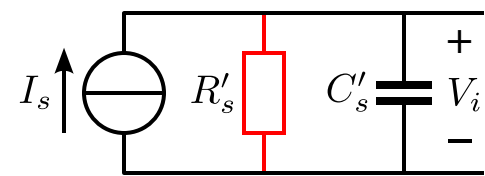
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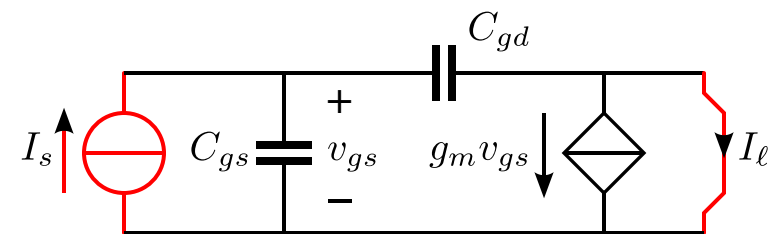
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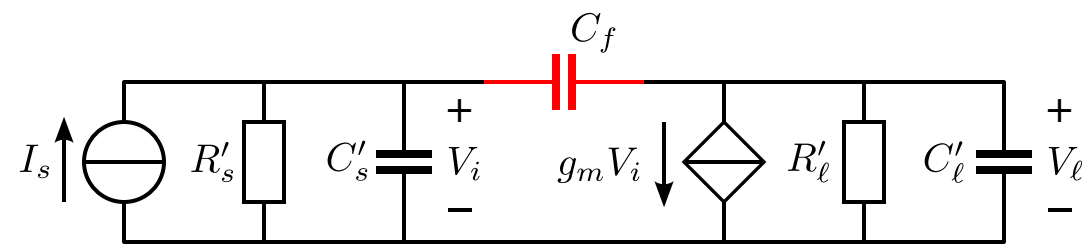


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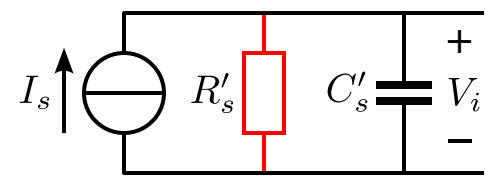
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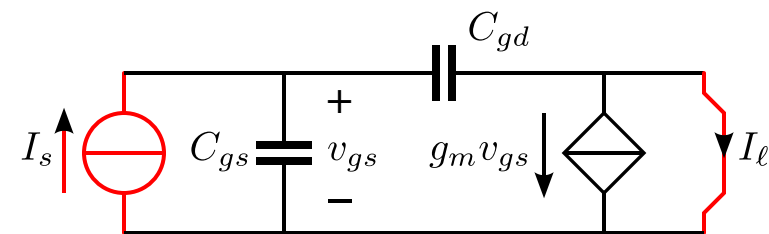
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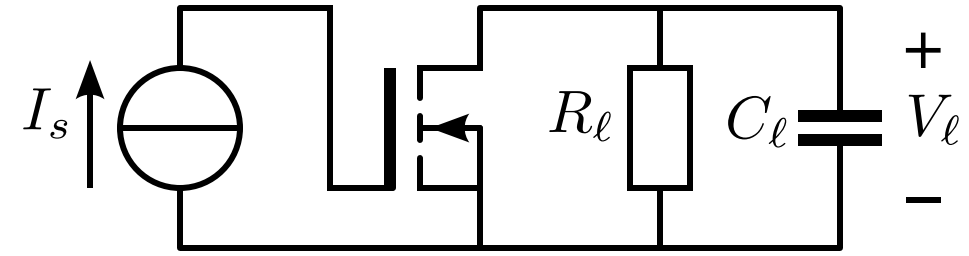
Miller-effect and cascode stage

Miller-effect and cascode stage

Biased, current-driven CS-stage with RC load

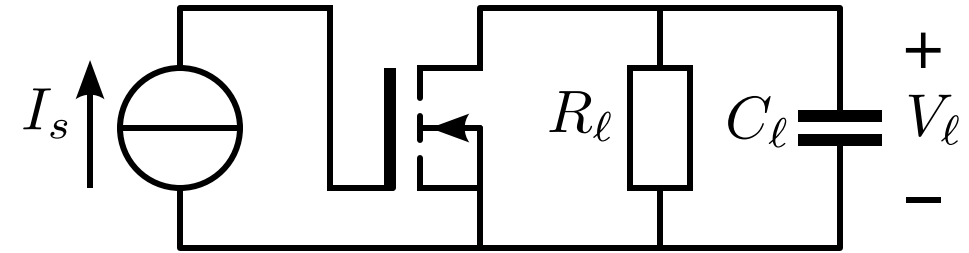
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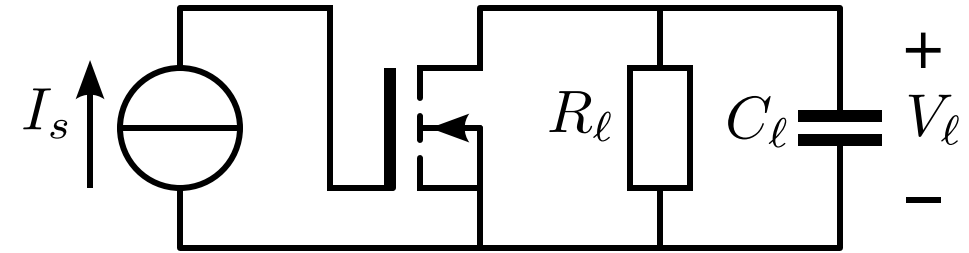
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Local capacitive feedback in the stage

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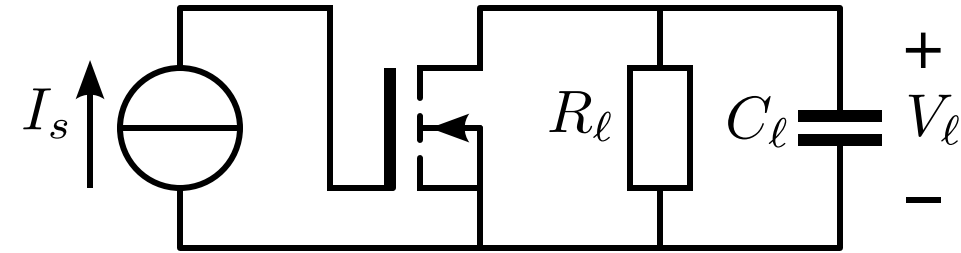


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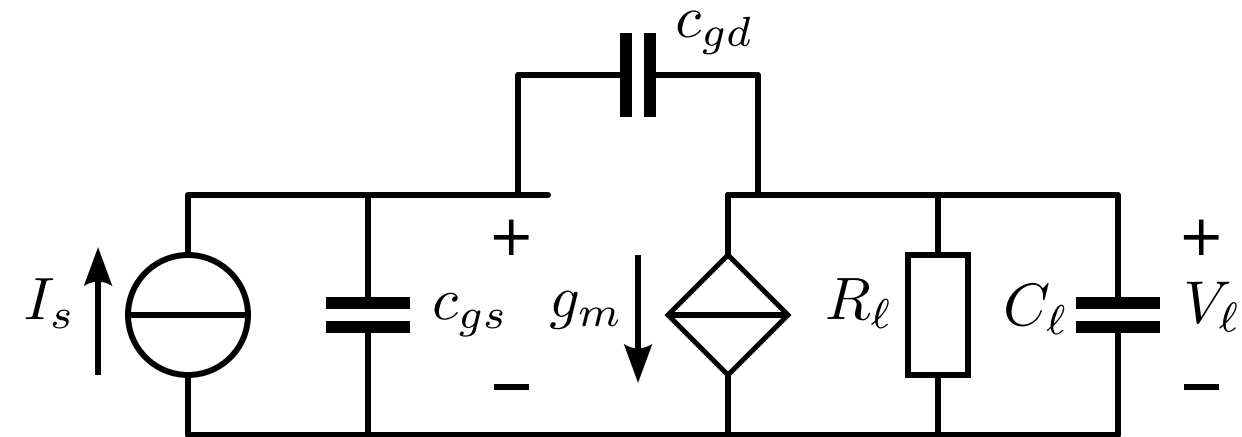
Small-signal diagram:

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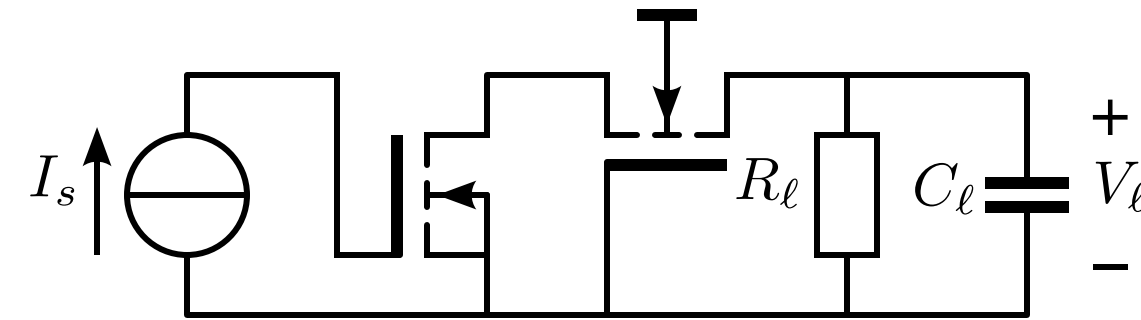
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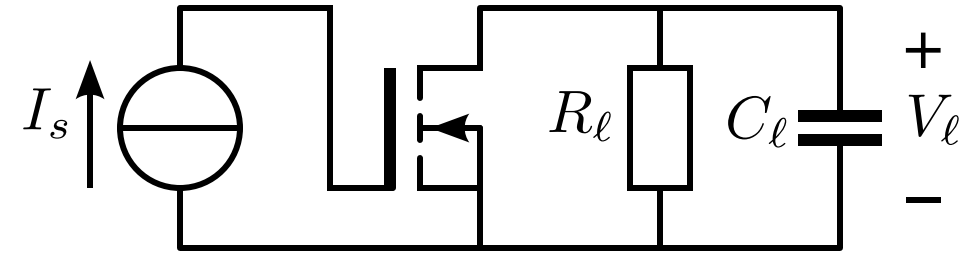
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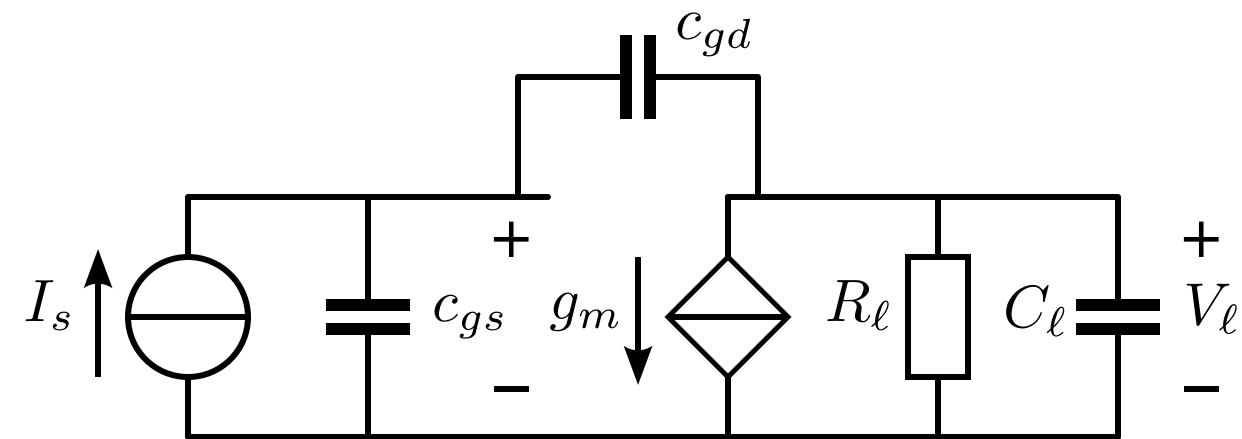
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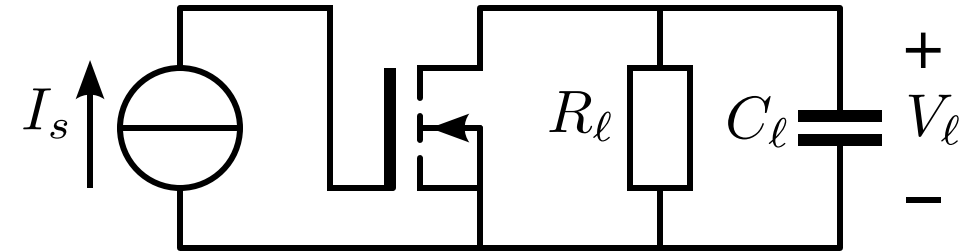
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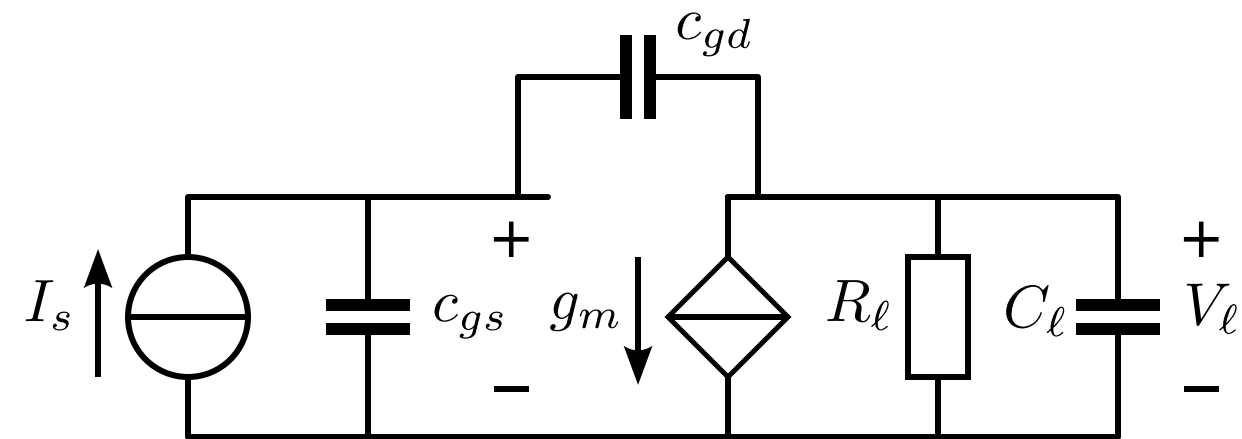
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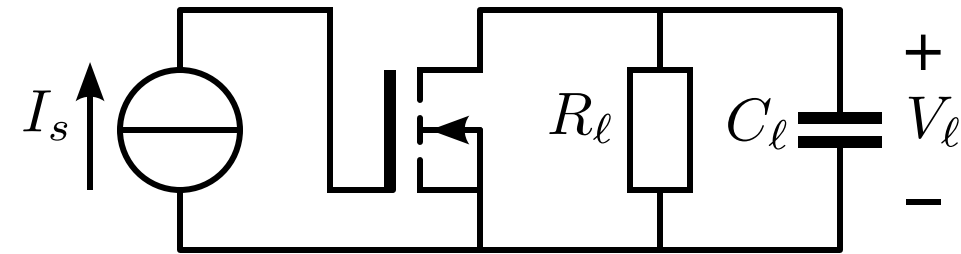


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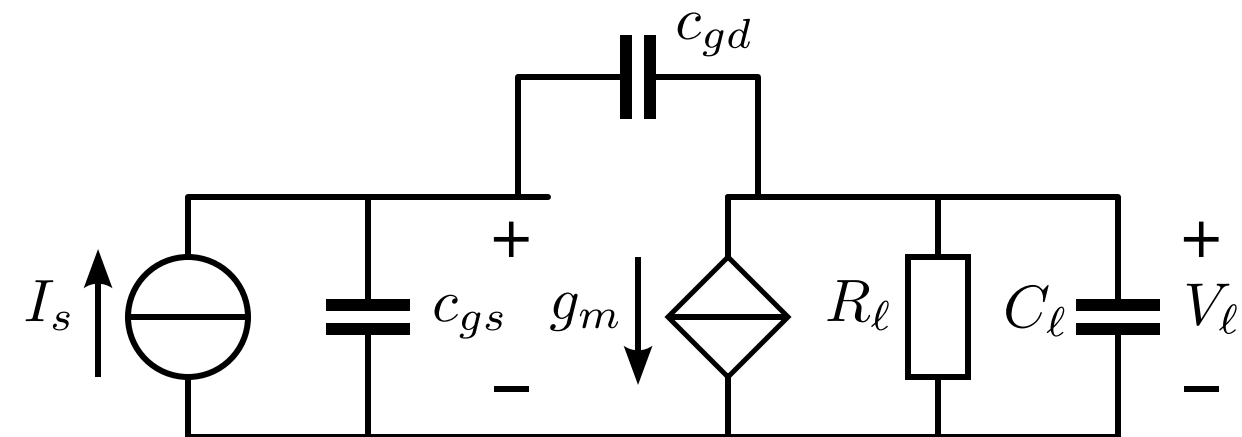
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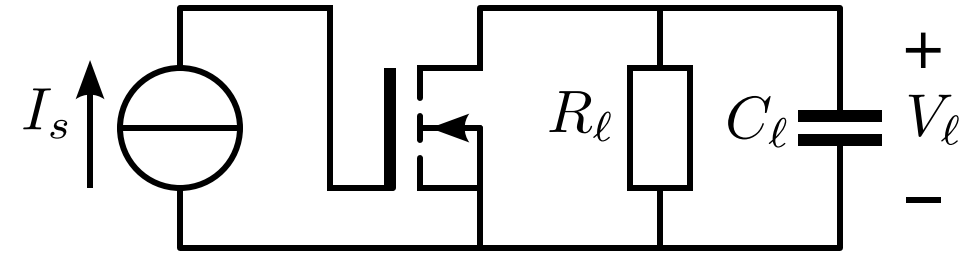
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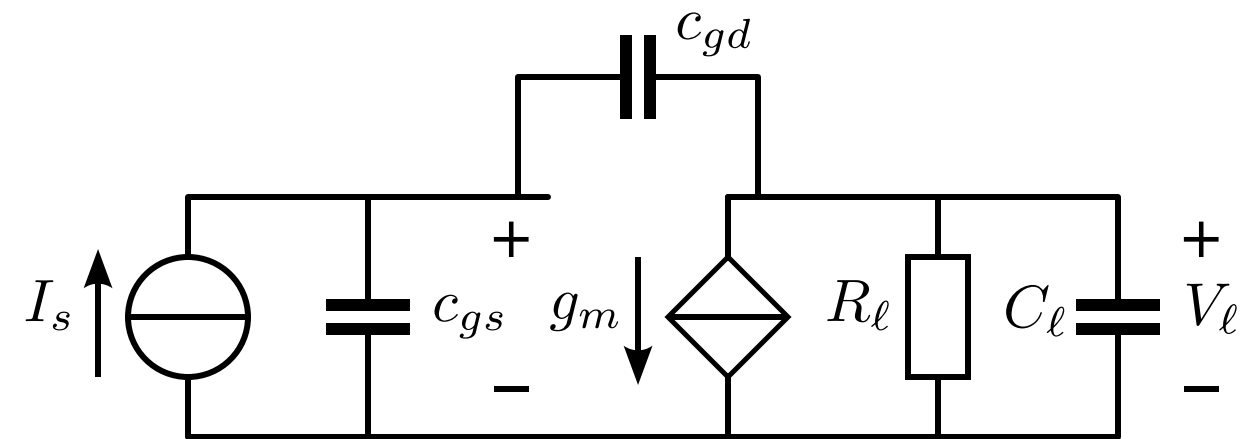
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Miller-effect and cascode stage

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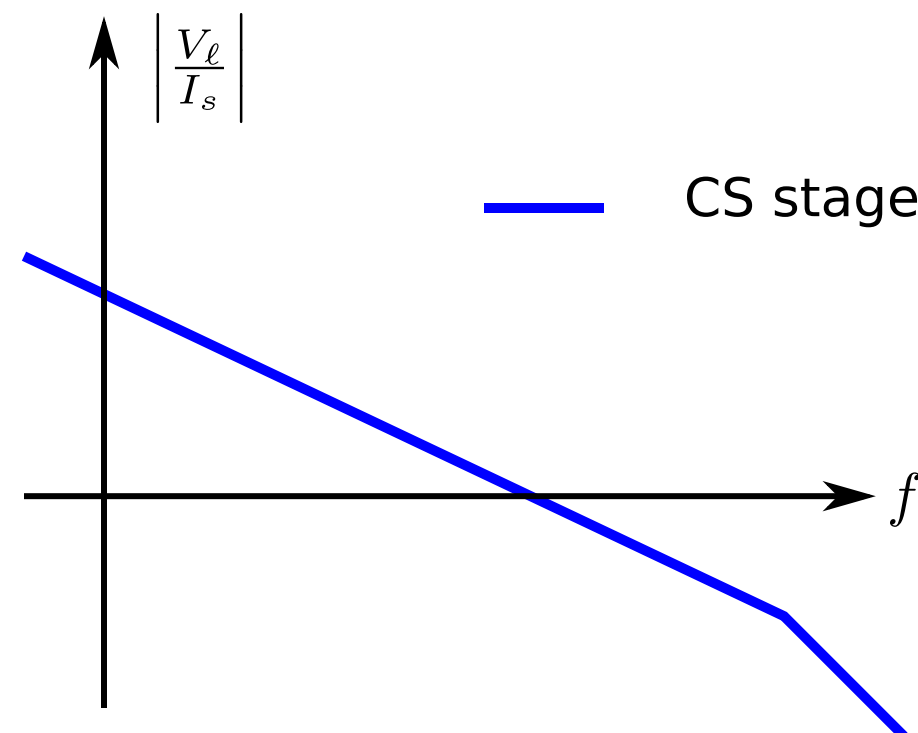
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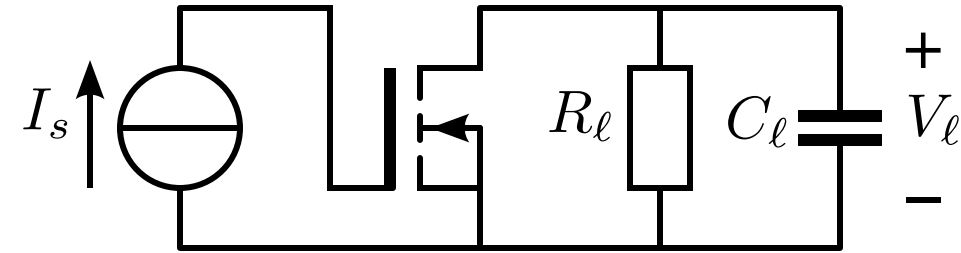
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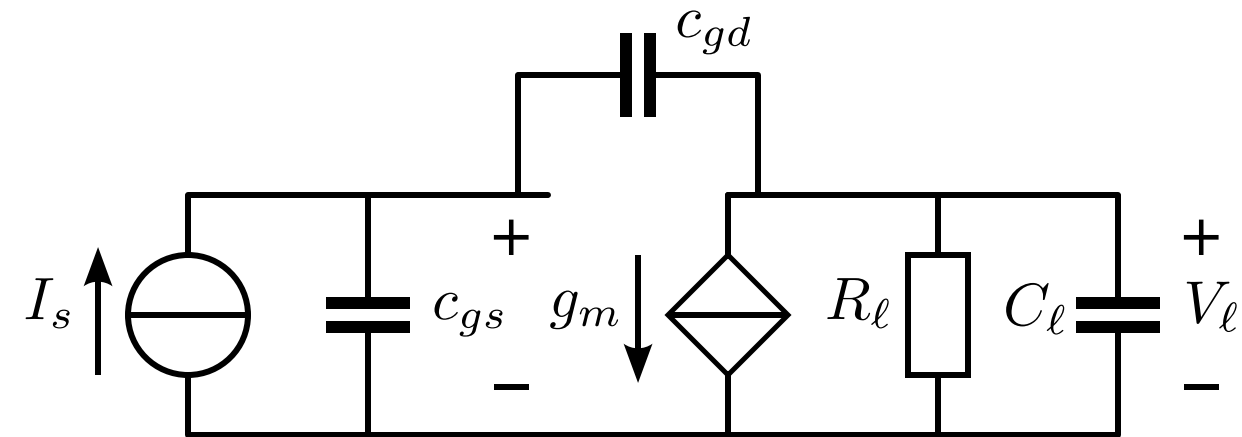
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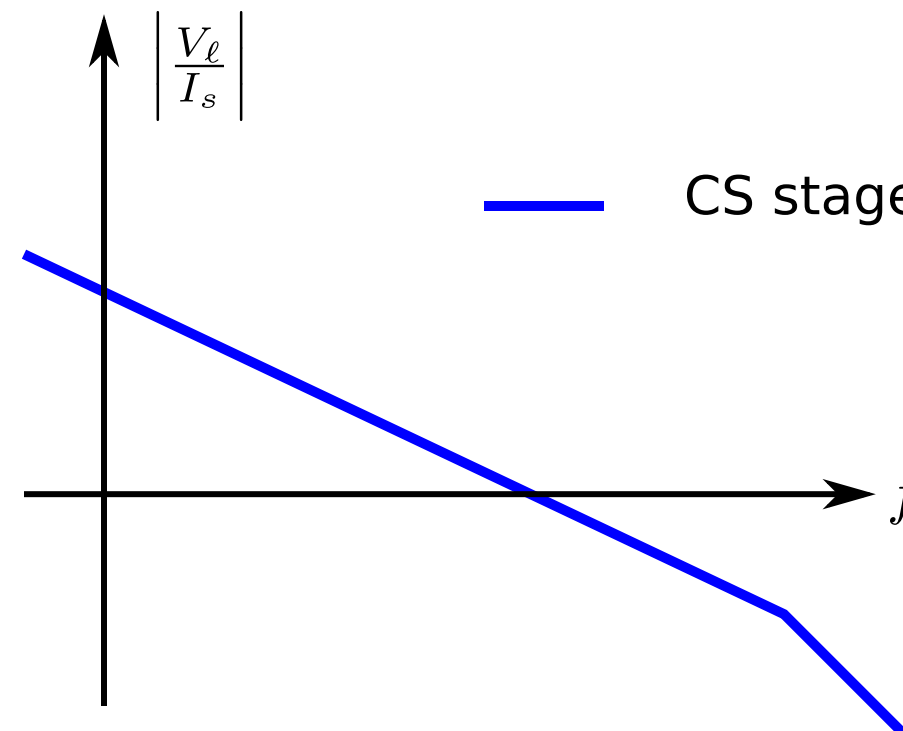
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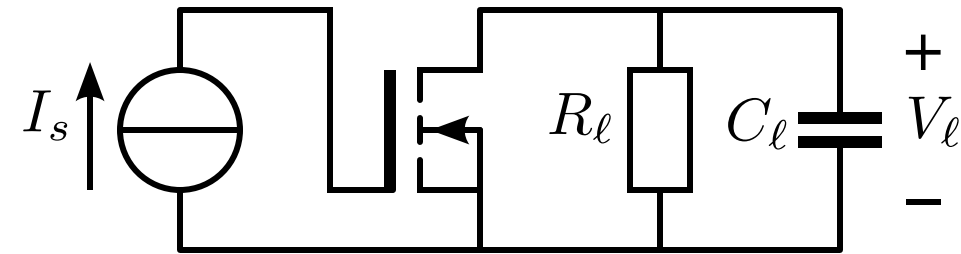
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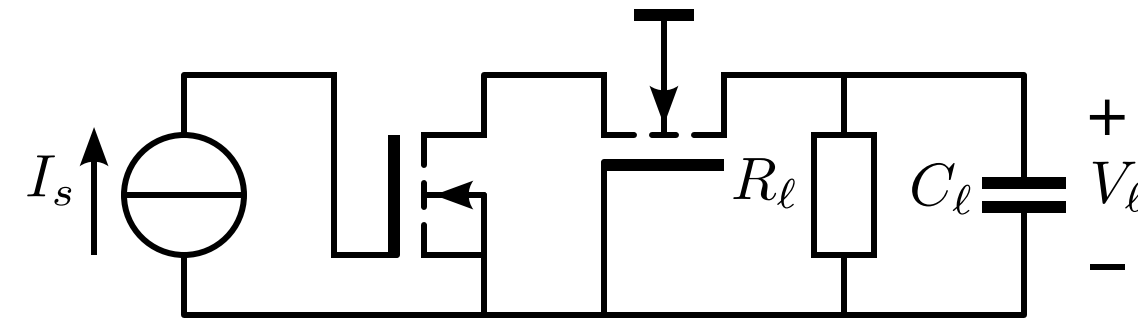


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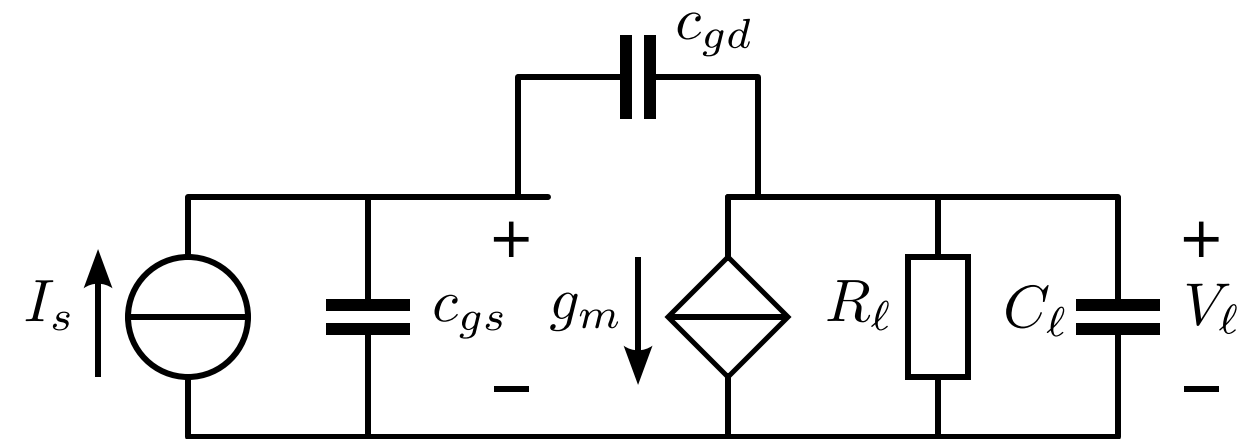
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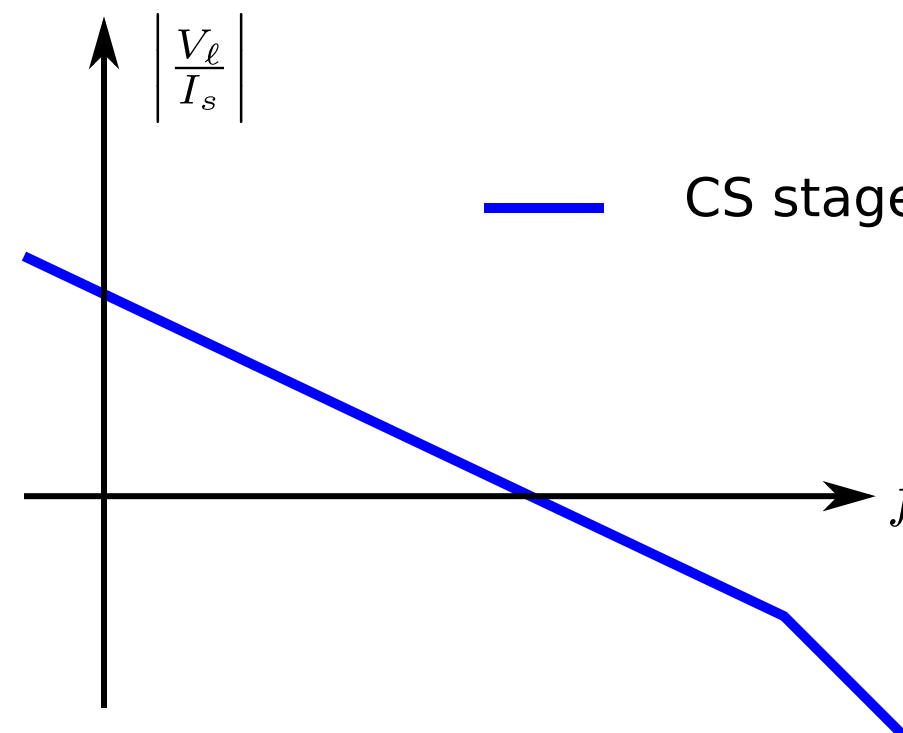
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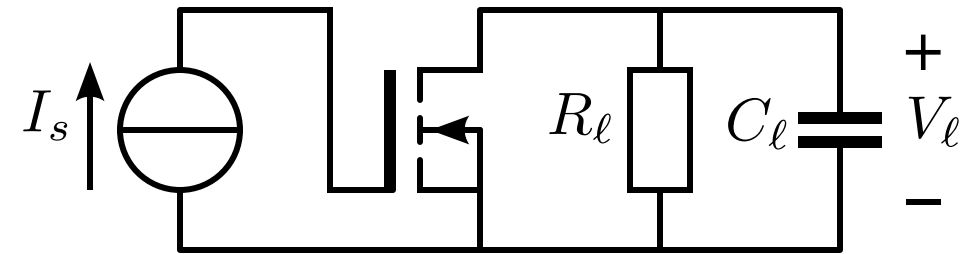
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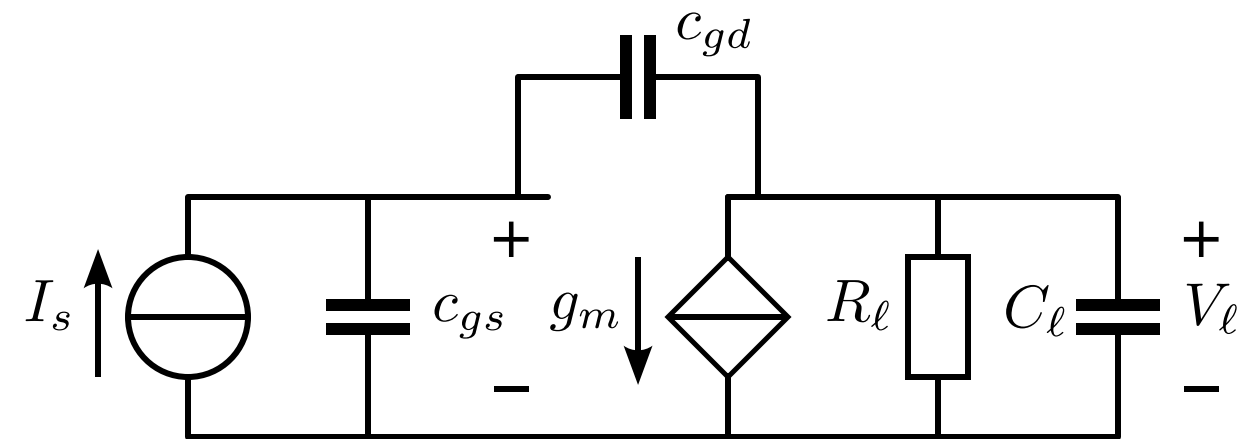


Miller-effect and cascode stage

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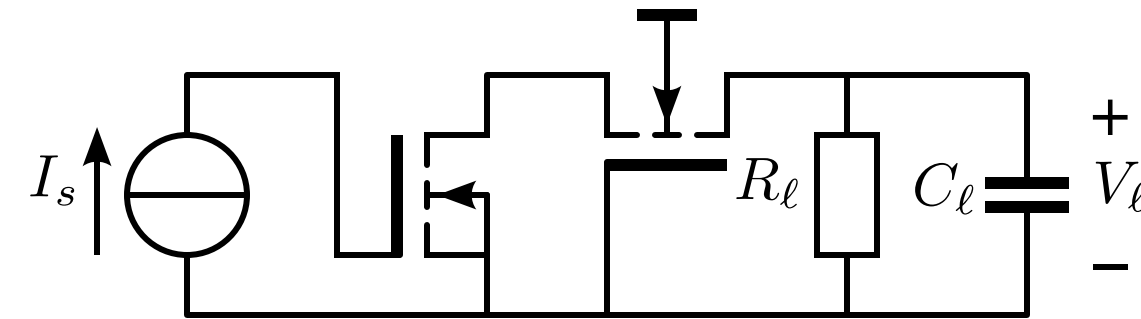


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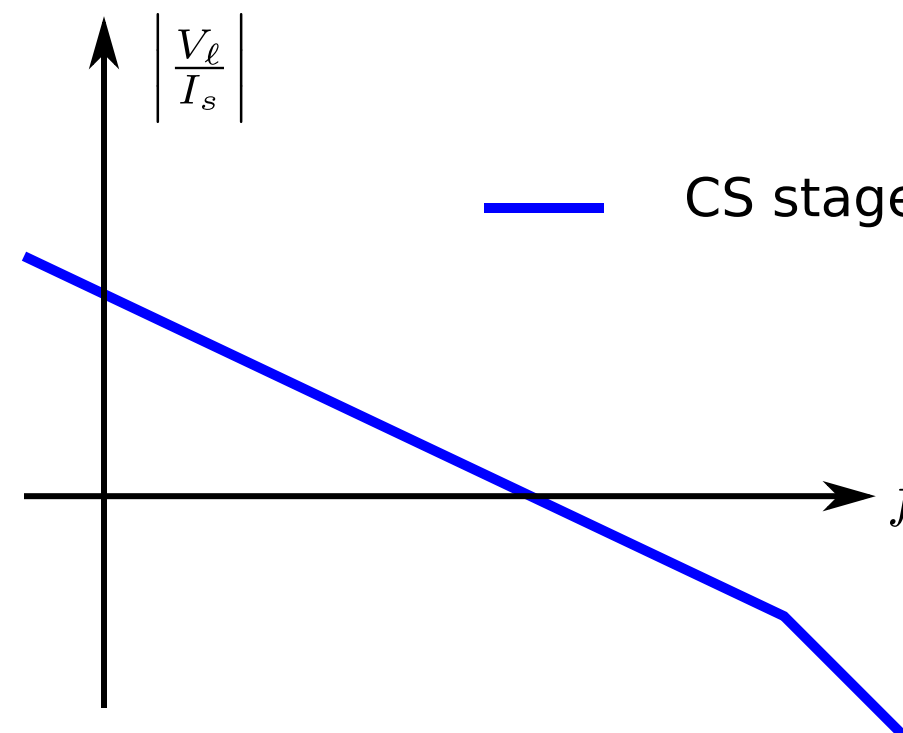
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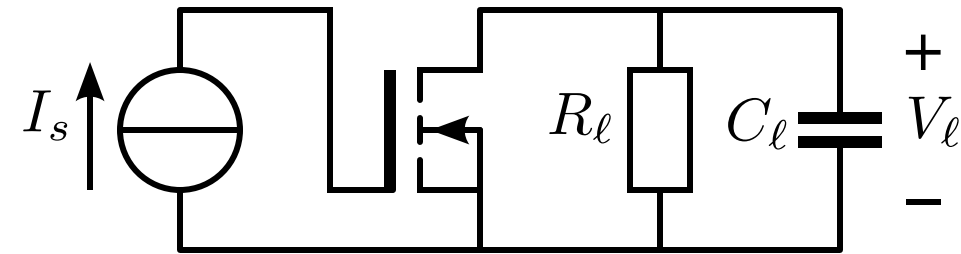


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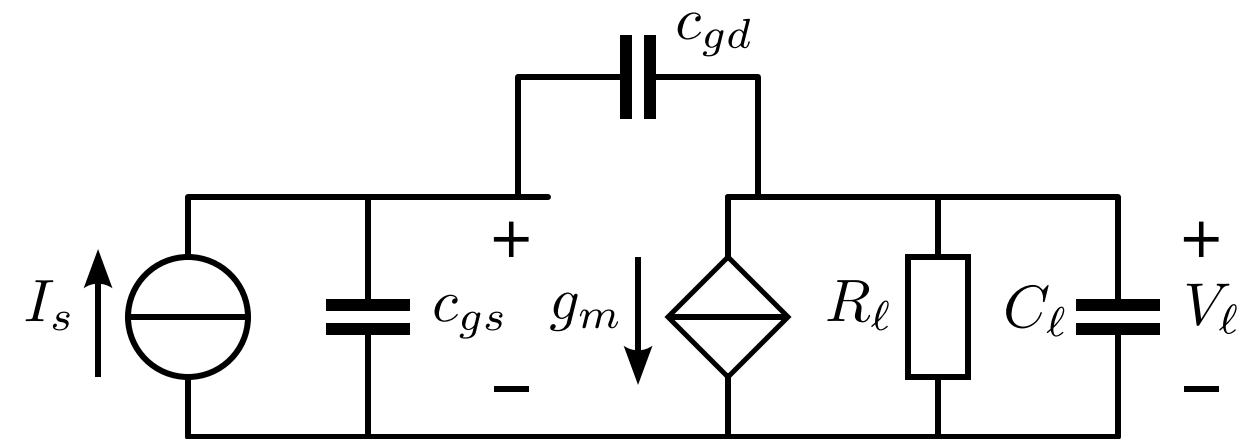


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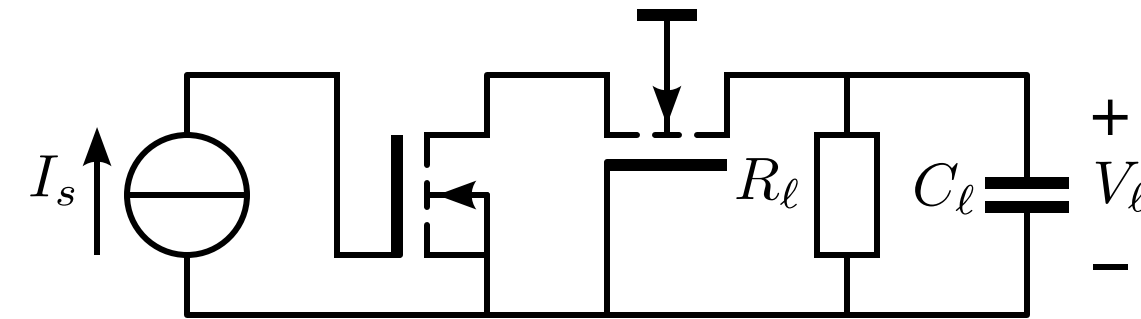


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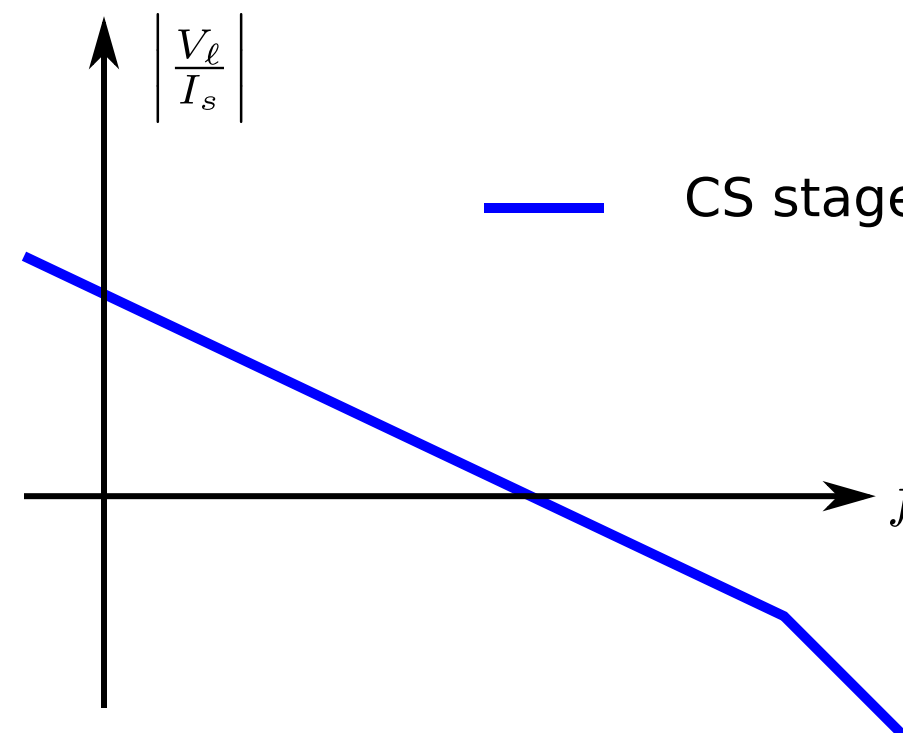
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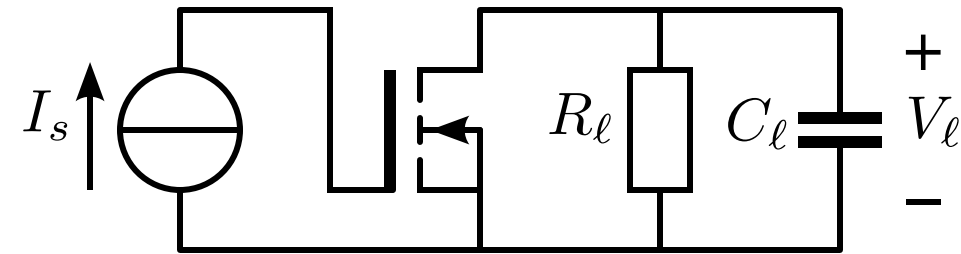


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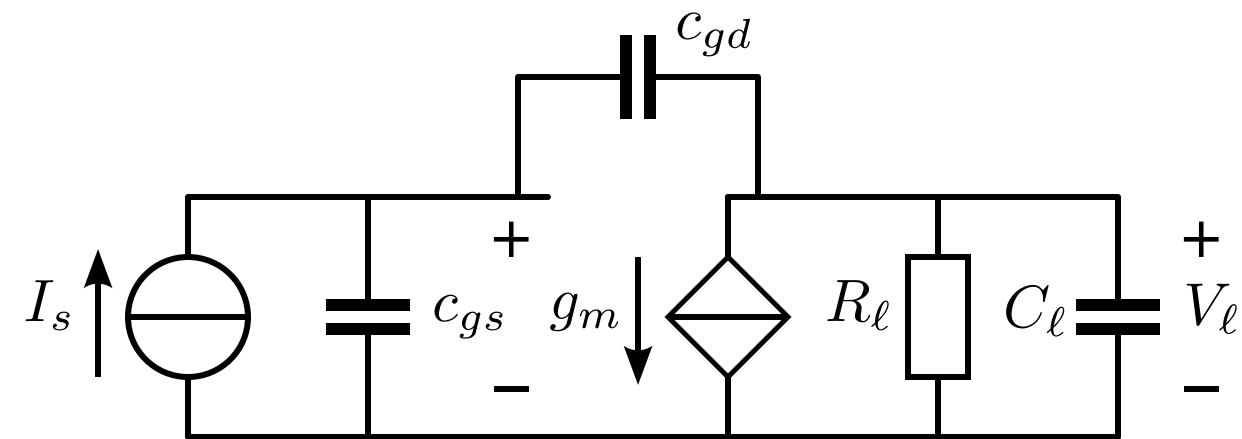


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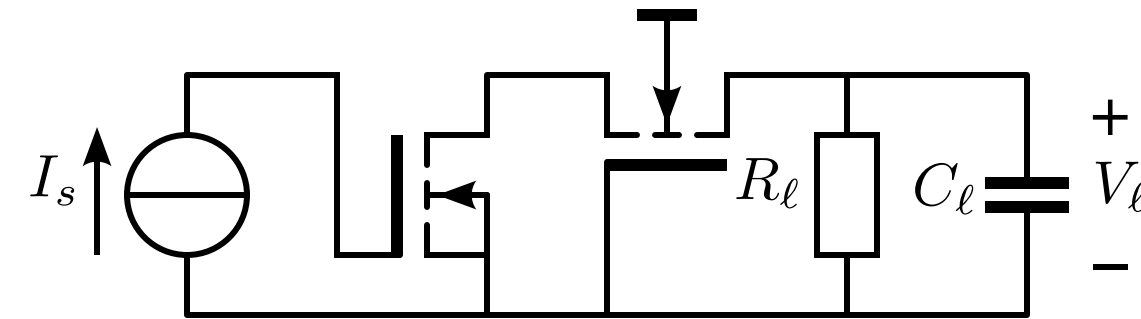


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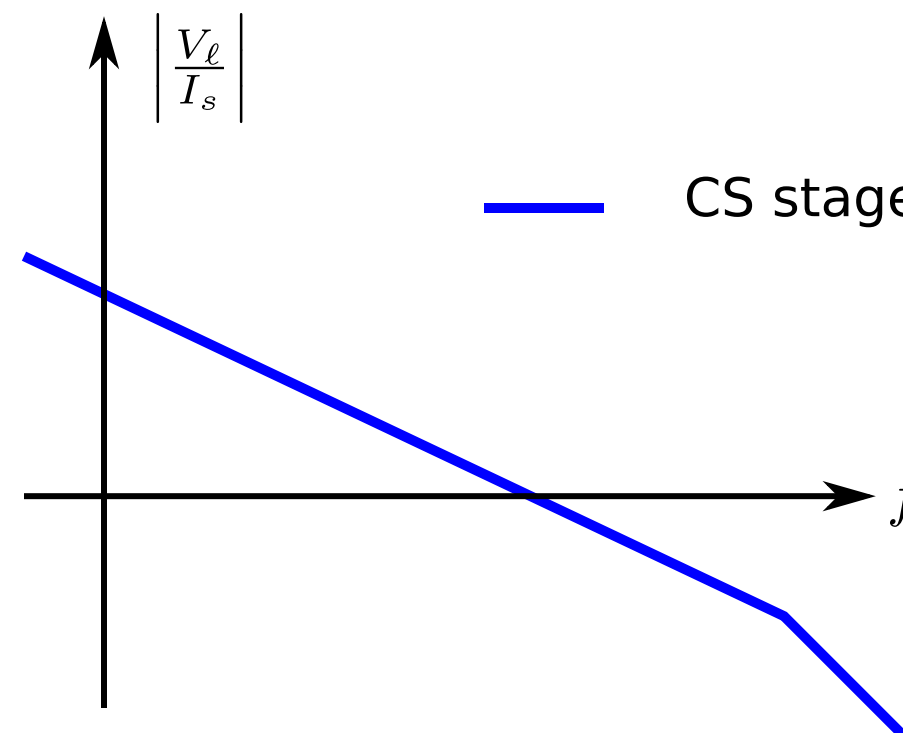
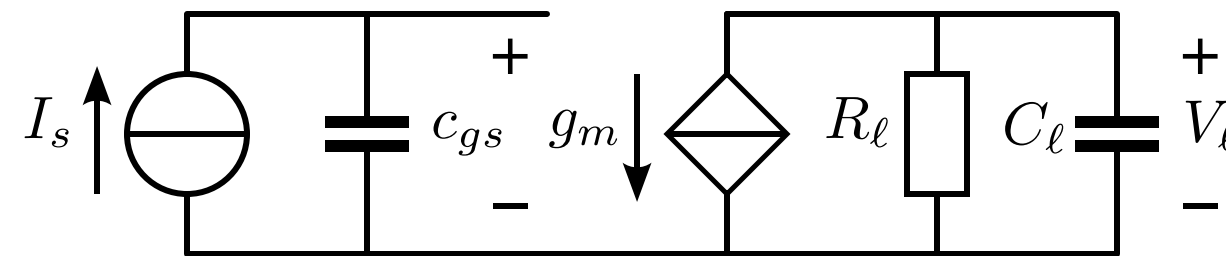
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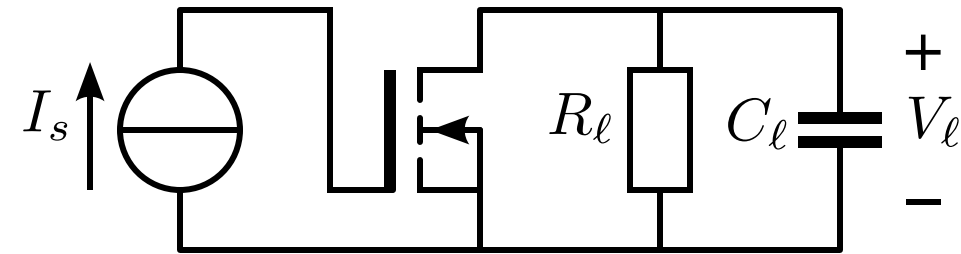


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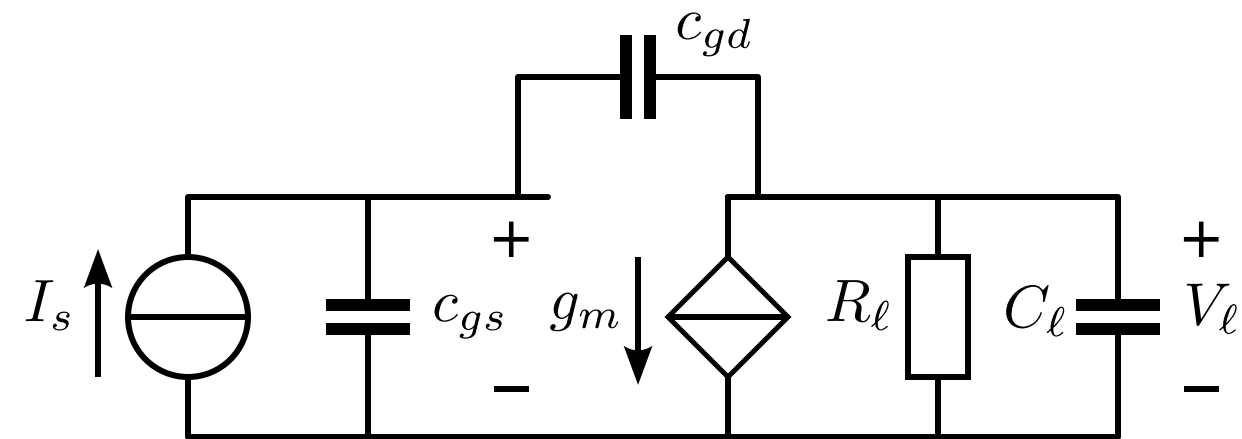


Miller-effect and cascode stage

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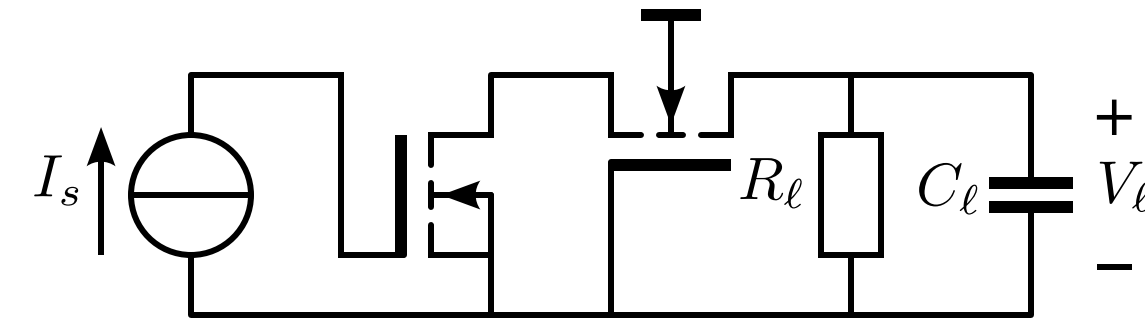


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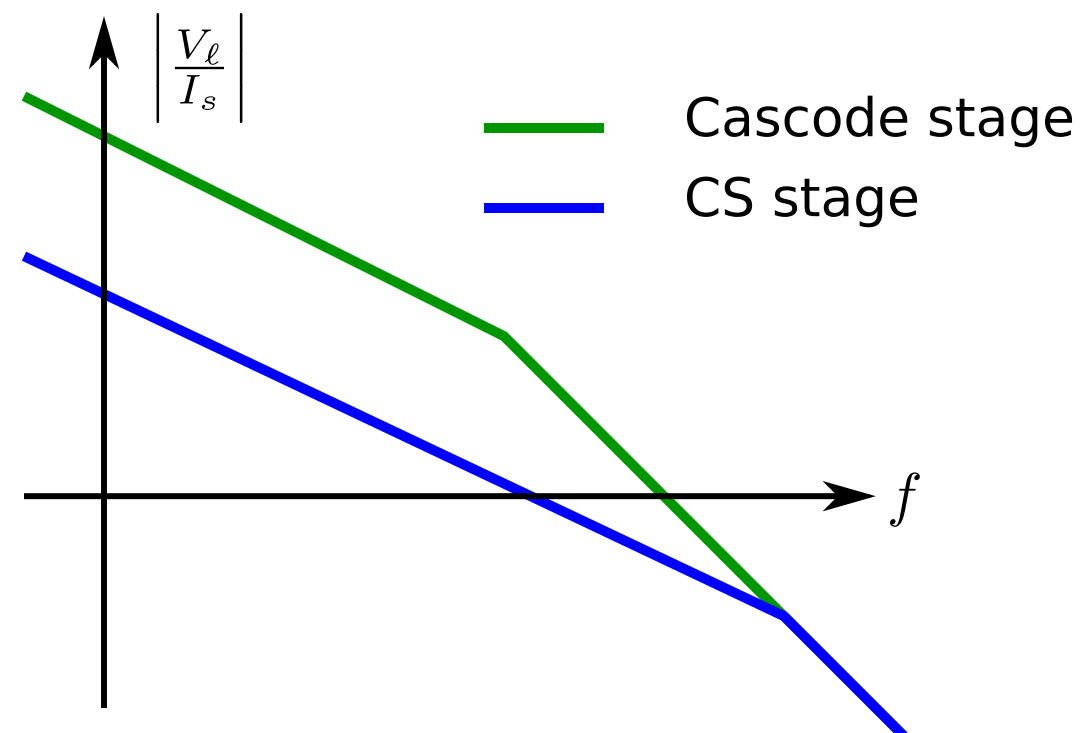
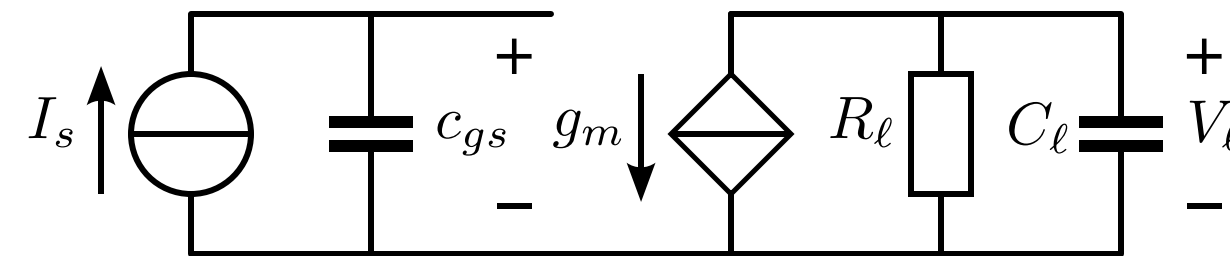
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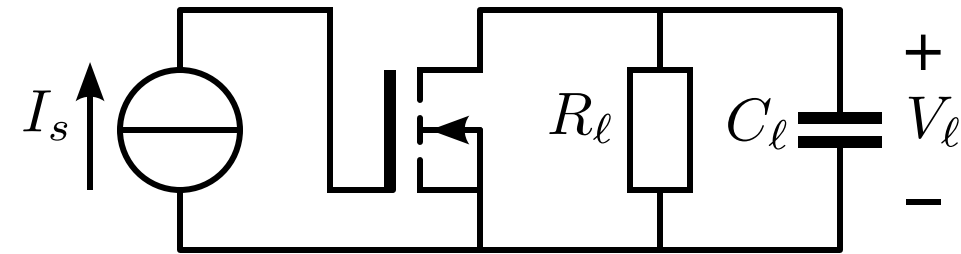


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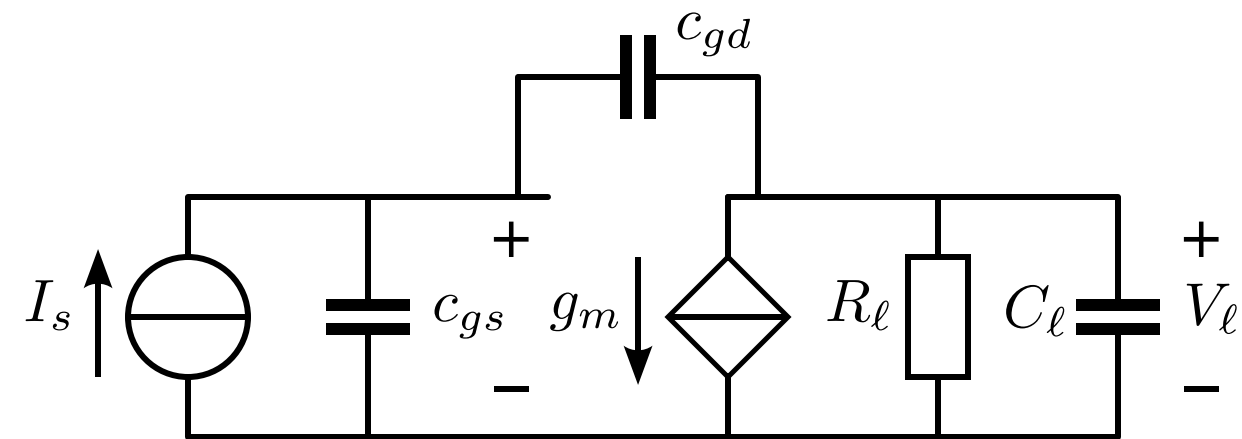


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Biased, current-driven CS-stage with RC load



Local capacitive feedback in the stage
Small-signal diagram:

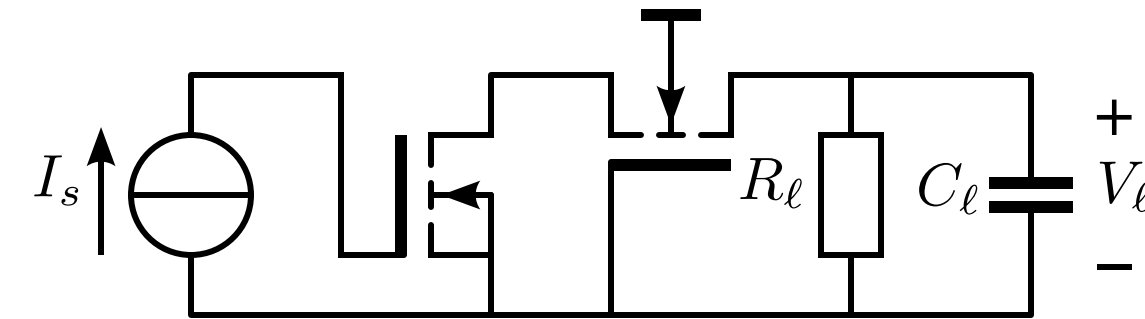


C_{gs} increases the sum of the poles:
pole-splitting

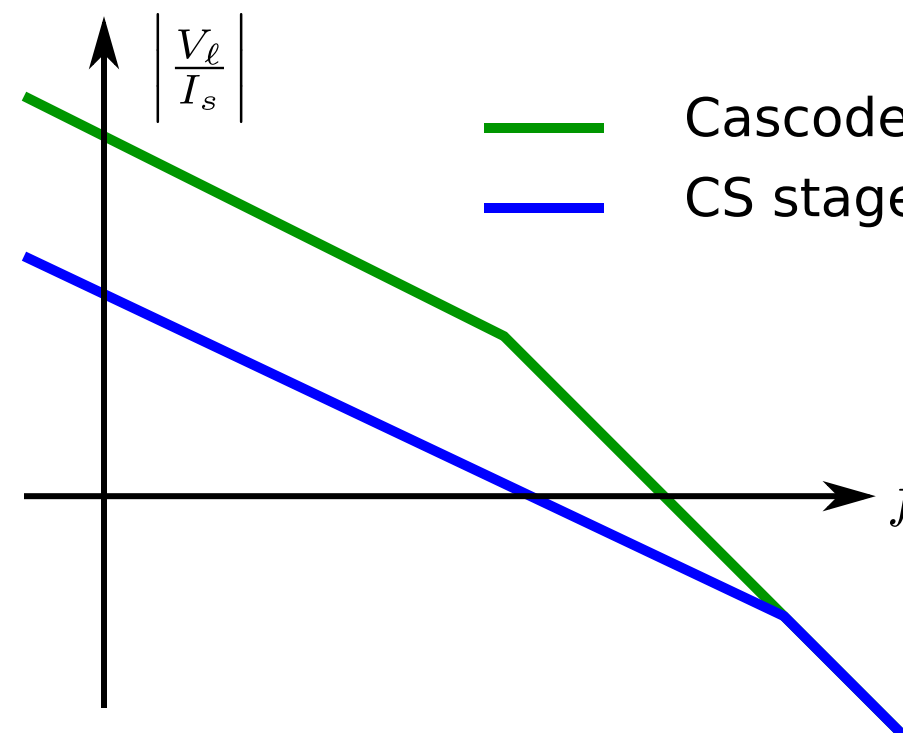
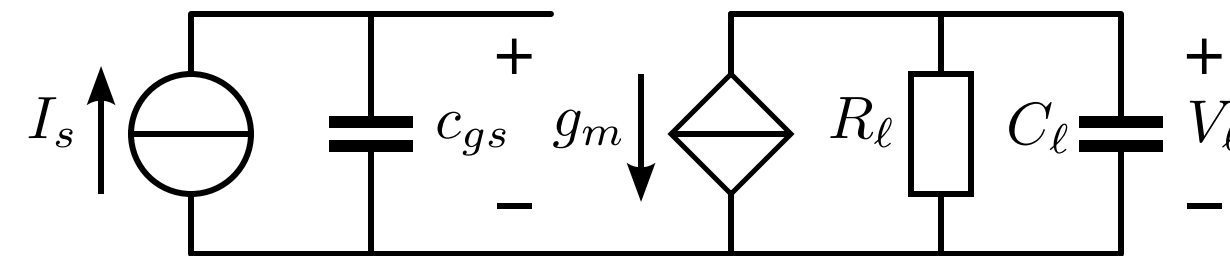
occurs if: $g_m R_l \gg 1$

product of the poles not affected
by C_{gd} if $C_{gd} \ll C_{gs}$ and $C_{gd} \ll C_l$

Biased, current-driven cascode stage with RC load



Strong reduction of local capacitive feedback in the stage
Small-signal diagram:

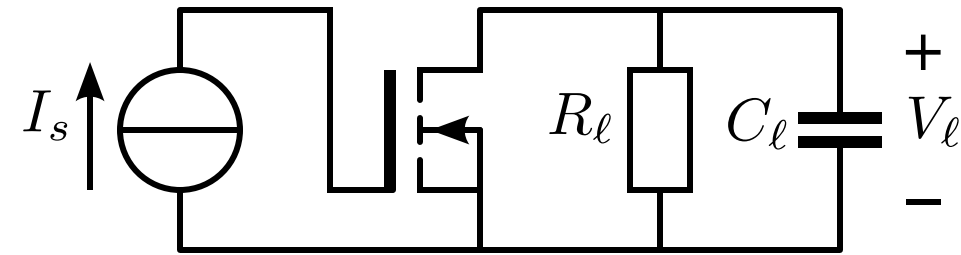


— Cascode stage
— CS stage

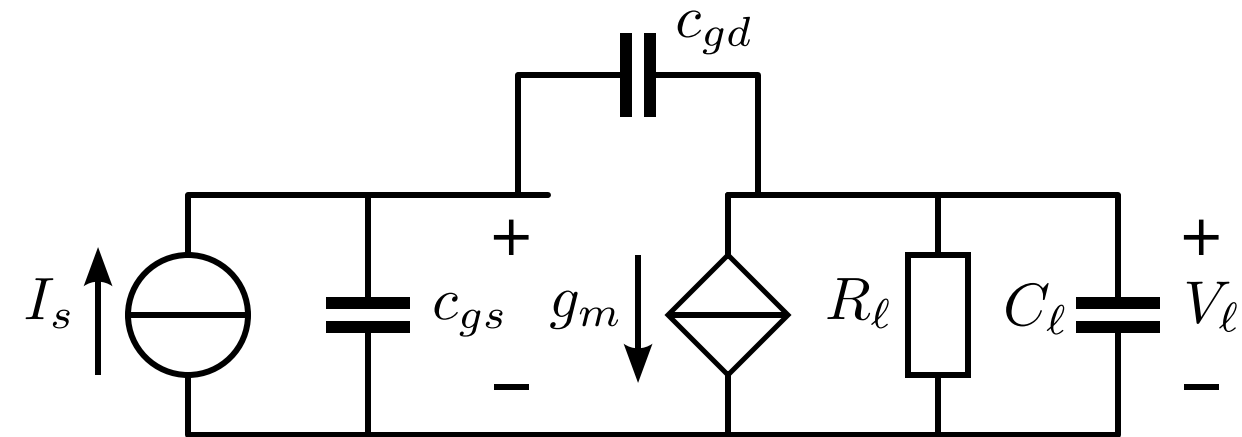
Cascode stage is considered a
single stage

Miller-effect and cascode stage

Biased, current-driven CS-stage with RC load



Local capacitive feedback in the stage
Small-signal diagram:

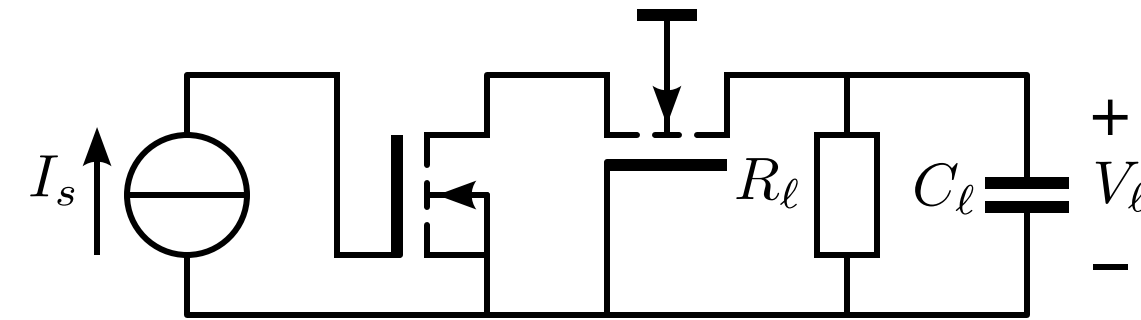


C_{gs} increases the sum of the poles:
pole-splitting

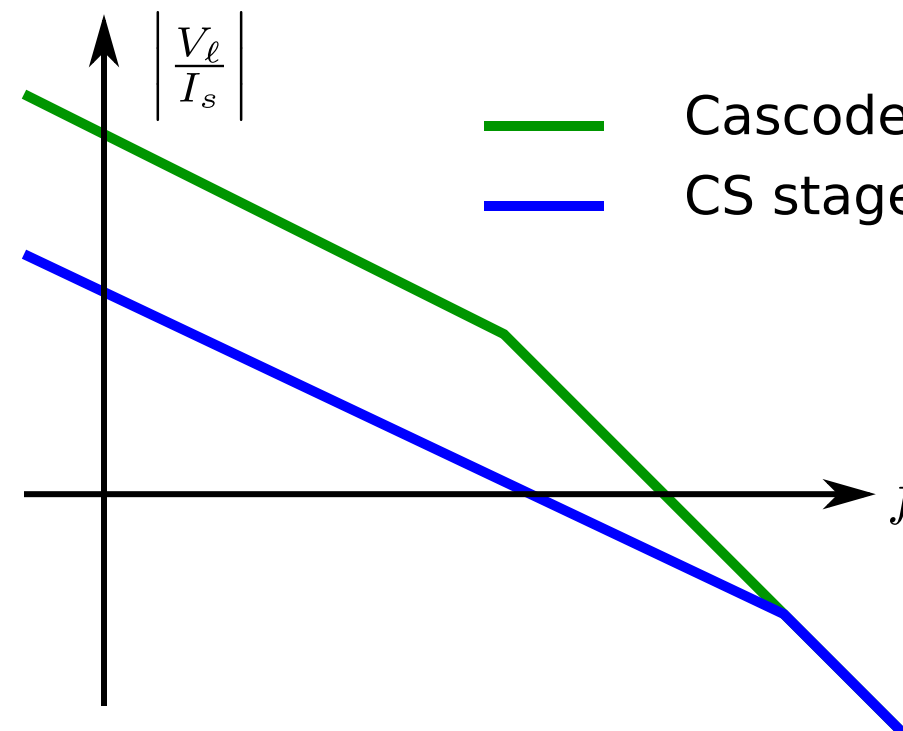
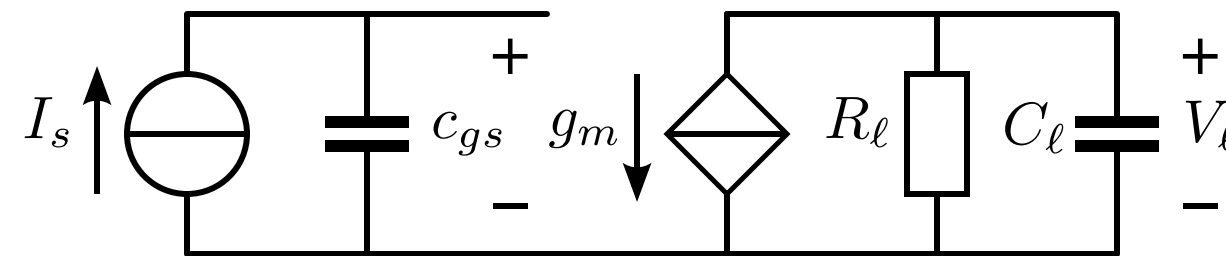
occurs if: $g_m R_l \gg 1$

product of the poles not affected
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Biased, current-driven cascode stage with RC load



Strong reduction of local capacitive feedback in the stage
Small-signal diagram:



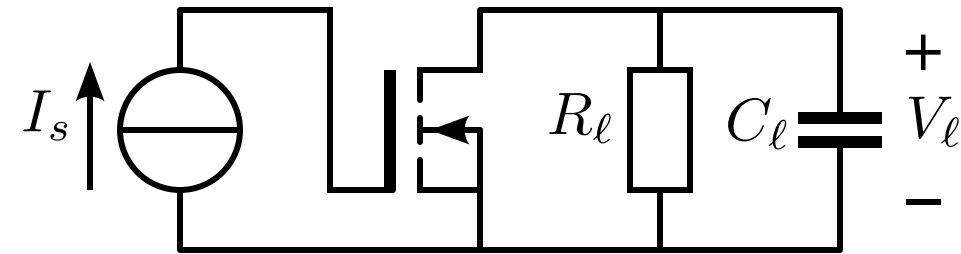
— Cascode stage
— CS stage

Cascode stage is considered a
single stage

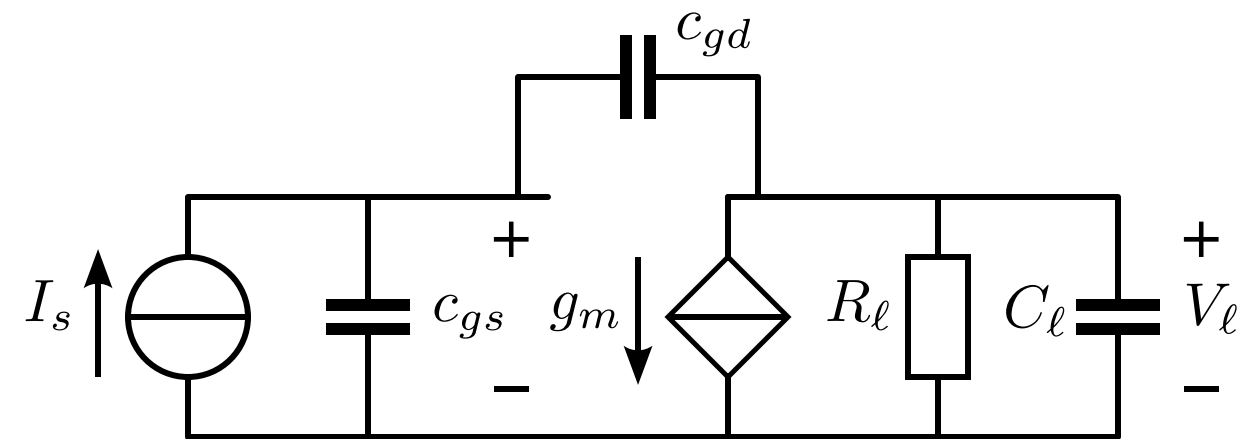
CG stage contributes a
(non dominant) pole at f_T
and unity current gain

Miller-effect and cascode stage

Biased, current-driven CS-stage with RC load



Local capacitive feedback in the stage
Small-signal diagram:

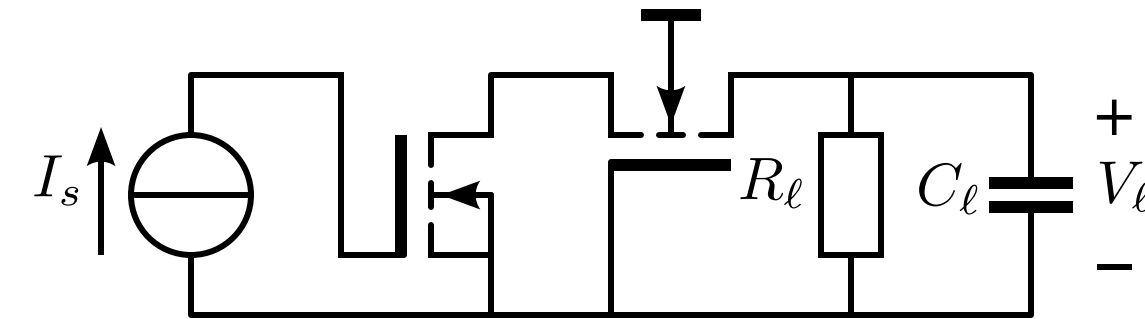


C_{gs} increases the sum of the poles:
pole-splitting

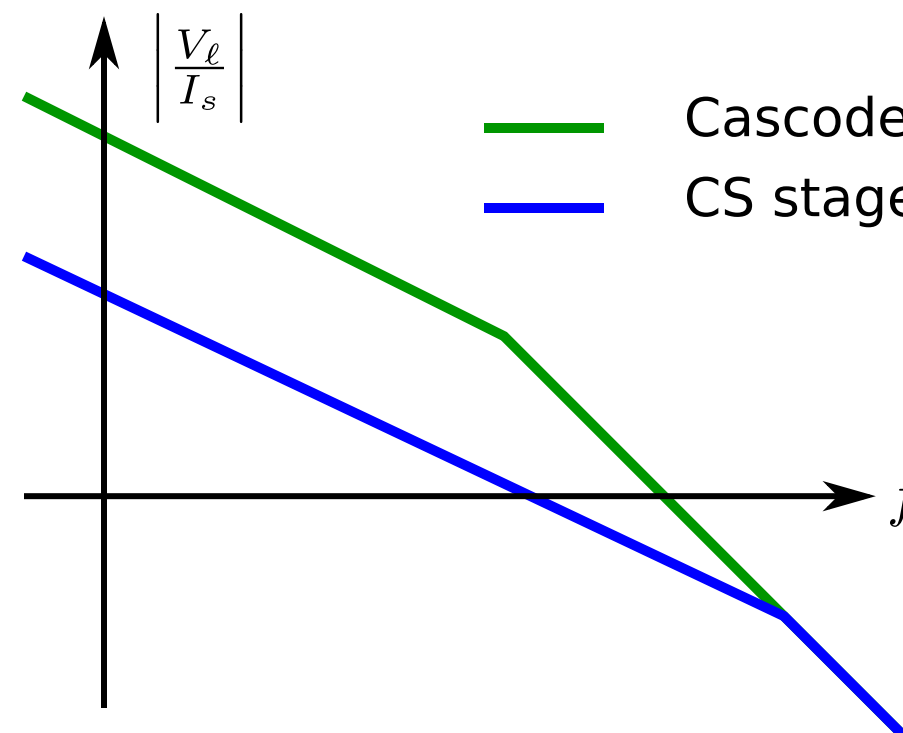
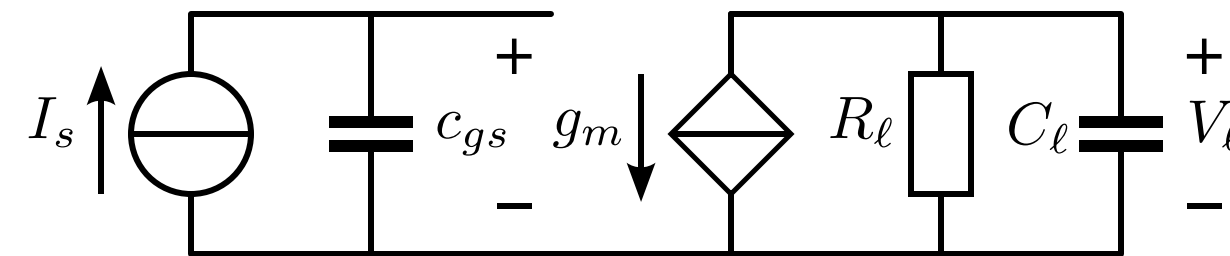
occurs if: $g_m R_l \gg 1$

product of the poles not affected
by C_{gd} if $C_{gd} \ll C_{gs}$ and $C_{gd} \ll C_l$

Biased, current-driven cascode stage with RC load



Strong reduction of local capacitive feedback in the stage
Small-signal diagram:



— Cascode stage
— CS stage

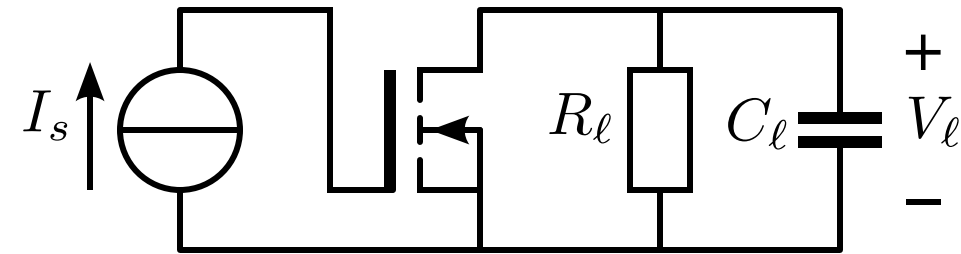
Cascode stage is considered a
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CG stage contributes a
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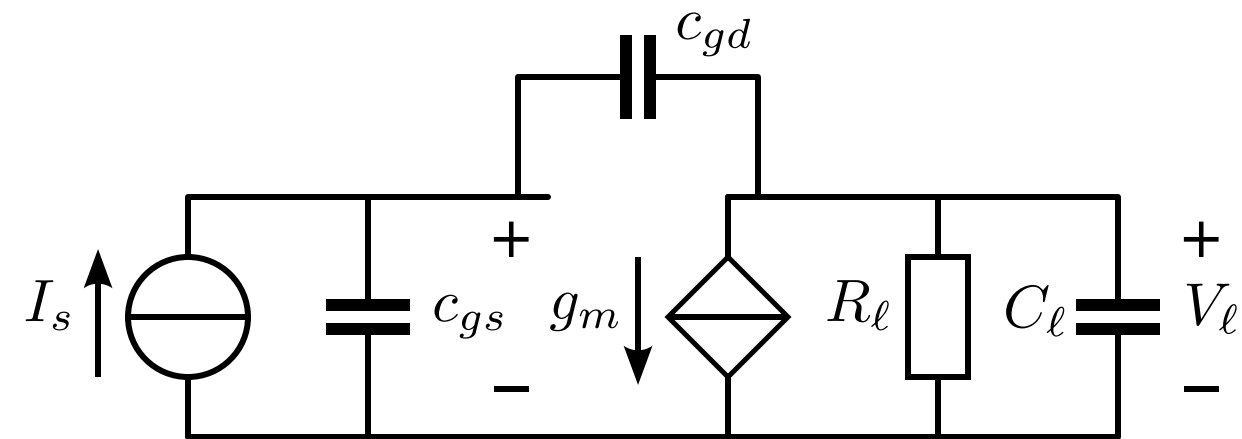
Uni-lateral stage

Miller-effect and cascode stage

Biased, current-driven CS-stage with RC load



Local capacitive feedback in the stage
Small-signal diagram:

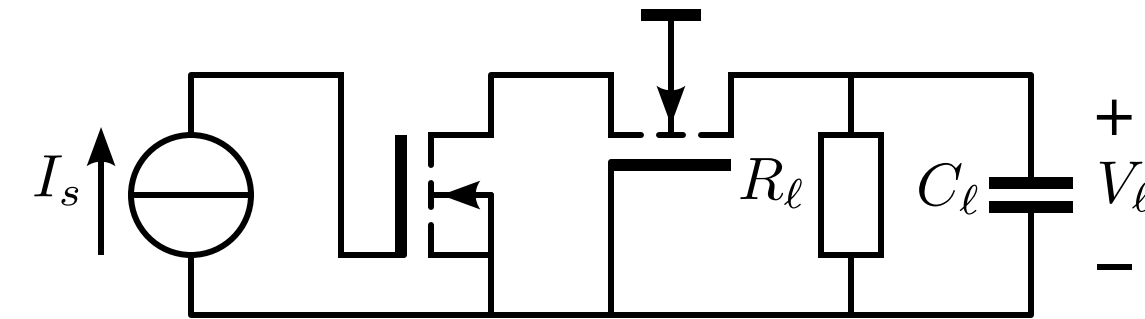


C_{gs} increases the sum of the poles:
pole-splitting

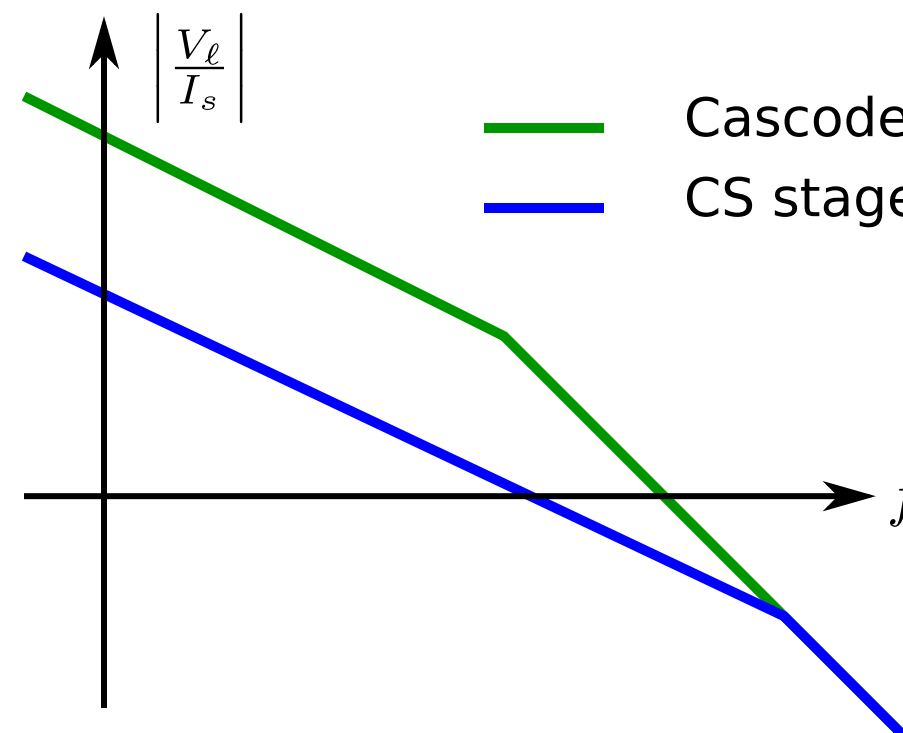
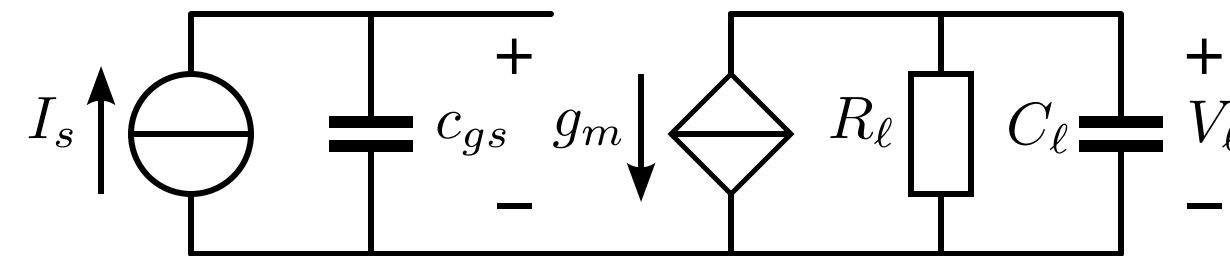
occurs if: $g_m R_l \gg 1$

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Biased, current-driven cascode stage with RC load



Strong reduction of local capacitive feedback in the stage
Small-signal diagram:



— Cascode stage
— CS stage

Cascode stage is considered a
single stage

CG stage contributes a
(non dominant) pole at f_T
and unity current gain

Uni-lateral stage

Structured Electronic Design

EE4109

Controller design:
Preferred stages

Anton J.M. Montagne

Uni-lateral stages with maximum LP product contribution

Uni-lateral stages with maximum LP product contribution

Three-terminal

Uni-lateral stages with maximum LP product contribution

Three-terminal

inverting

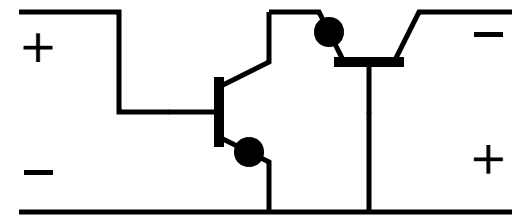
CS-CG cascode stage

Uni-lateral stages with maximum LP product contribution

Three-terminal

inverting

CS-CG cascode stage

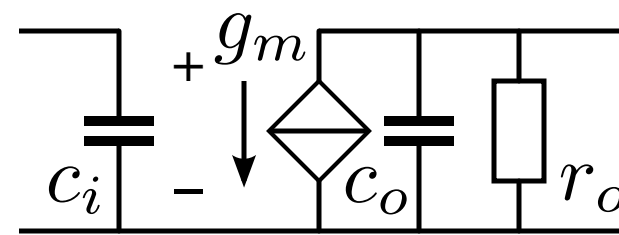
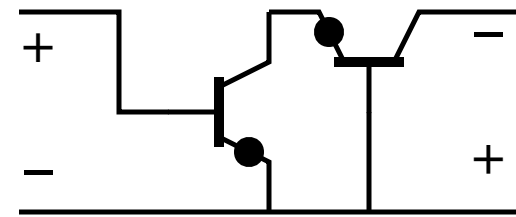


Uni-lateral stages with maximum LP product contribution

Three-terminal

inverting

CS-CG cascode stage

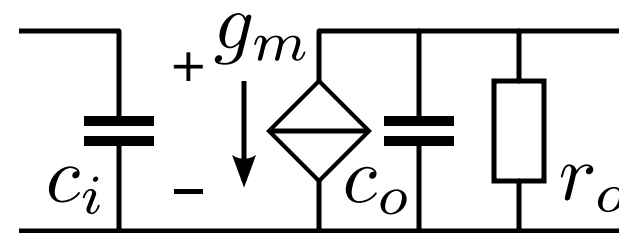
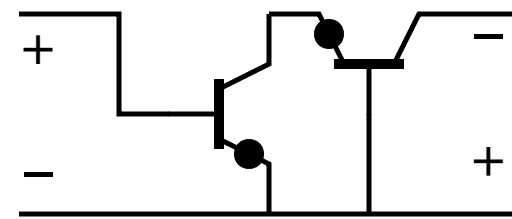


Uni-lateral stages with maximum LP product contribution

Three-terminal

inverting
CS-CG cascode stage

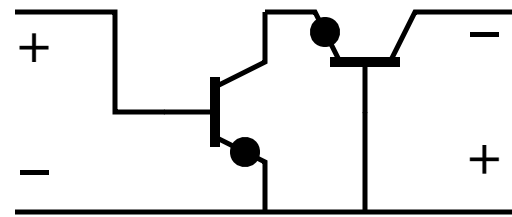
non-inverting
CD-CG cascode stage



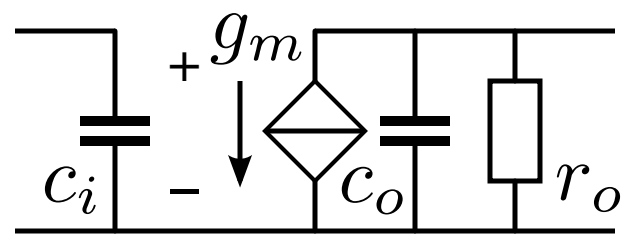
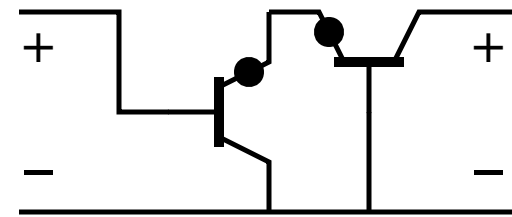
Uni-lateral stages with maximum LP product contribution

Three-terminal

inverting
CS-CG cascode stage



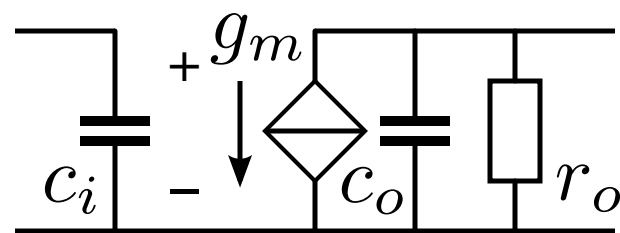
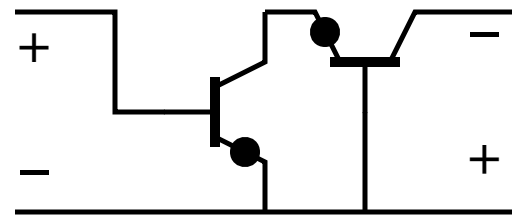
non-inverting
CD-CG cascode stage



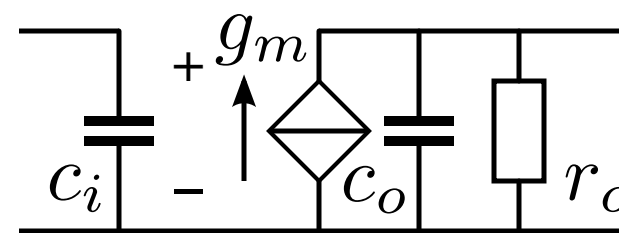
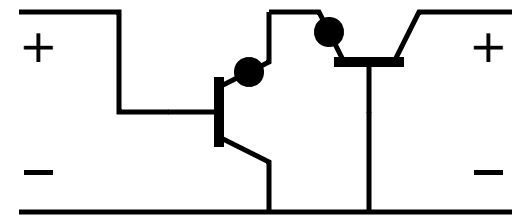
Uni-lateral stages with maximum LP product contribution

Three-terminal

inverting
CS-CG cascode stage



non-inverting
CD-CG cascode stage



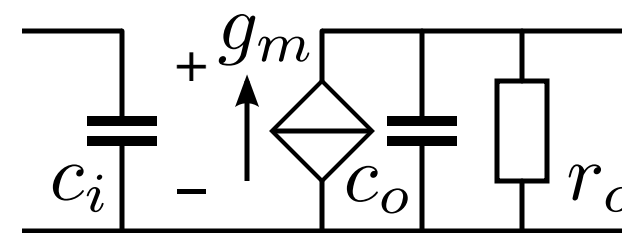
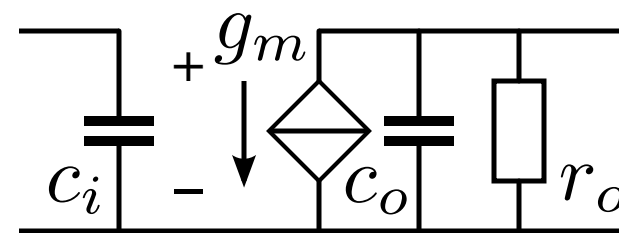
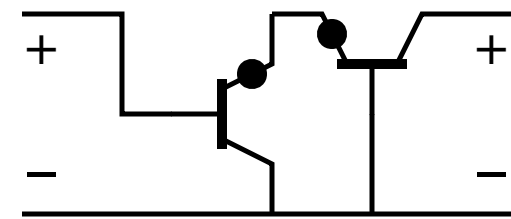
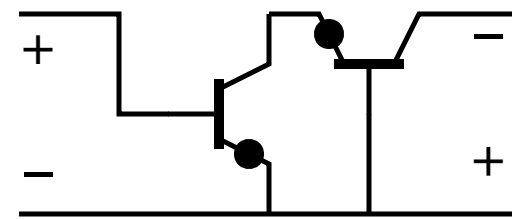
Uni-lateral stages with maximum LP product contribution

Three-terminal

Four-terminal

inverting
CS-CG cascode stage

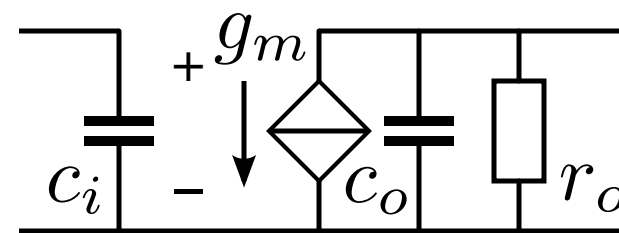
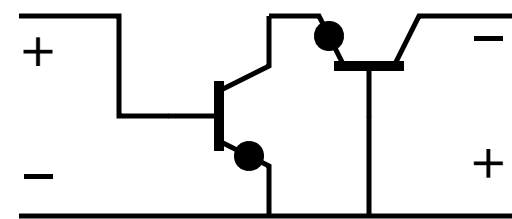
non-inverting
CD-CG cascode stage



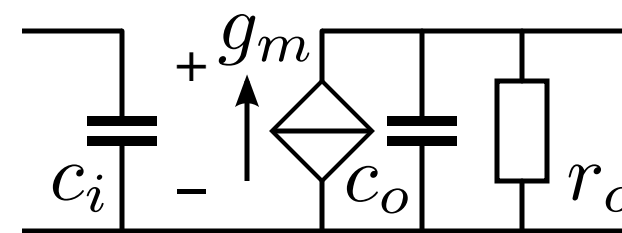
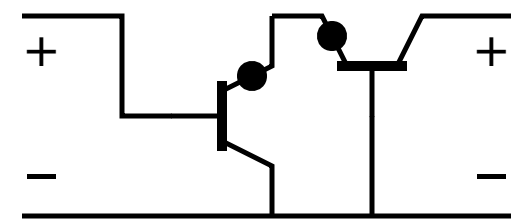
Uni-lateral stages with maximum LP product contribution

Three-terminal

inverting
CS-CG cascode stage



non-inverting
CD-CG cascode stage



Four-terminal

differential pair
cascode stage

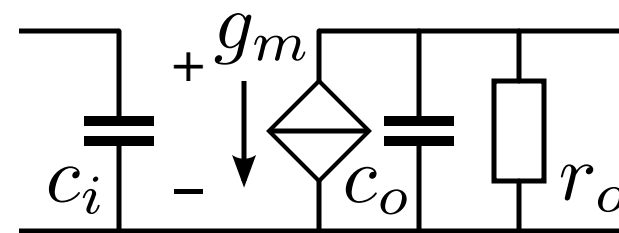
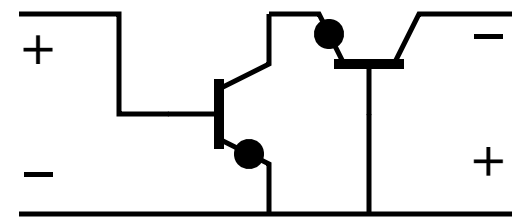
$$g_m = g_{m_1} \quad C_i = C_{gs_1} + C_{gd_1} \quad C_o = C_{gd_2} + C_{db_2}$$

$$\text{Current driven: } r_o = (1 + g_{m_1} r_{o_1}) r_{o_2}$$

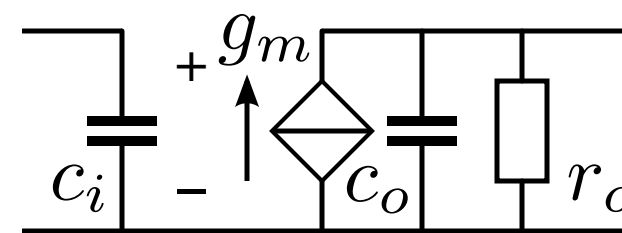
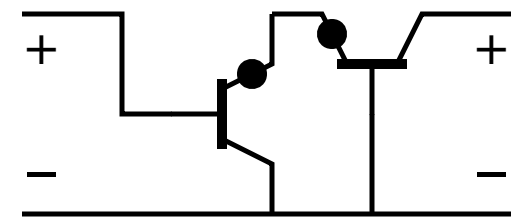
Uni-lateral stages with maximum LP product contribution

Three-terminal

inverting
CS-CG cascode stage

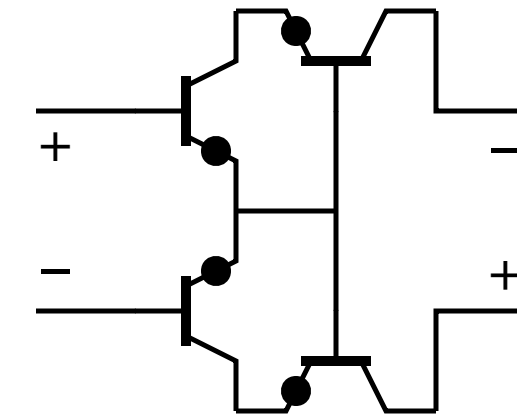


non-inverting
CD-CG cascode stage



Four-terminal

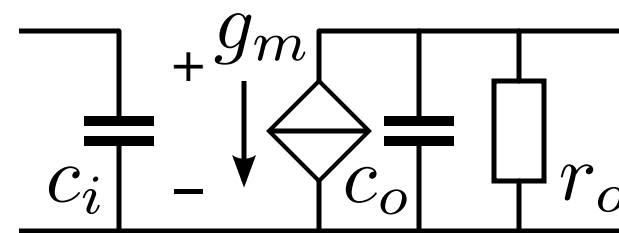
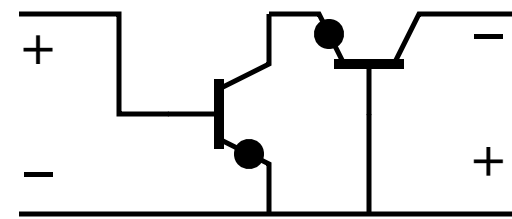
differential pair
cascode stage



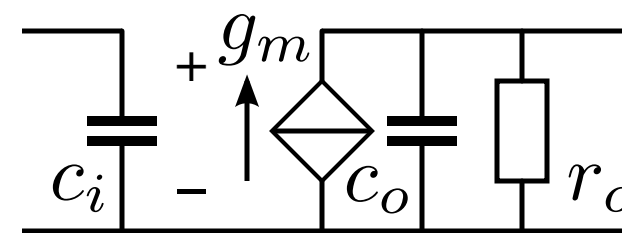
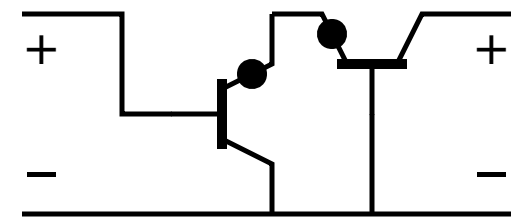
Uni-lateral stages with maximum LP product contribution

Three-terminal

inverting
CS-CG cascode stage

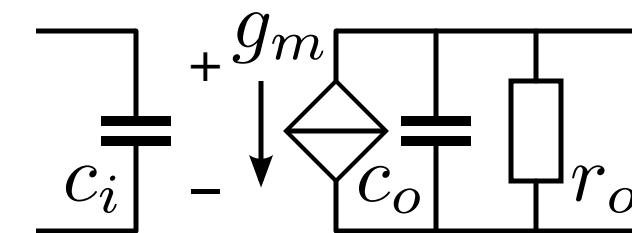
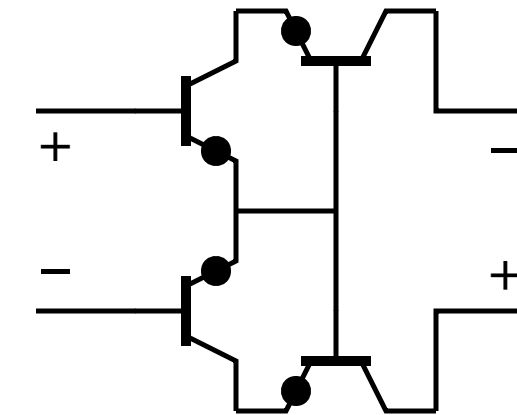


non-inverting
CD-CG cascode stage



Four-terminal

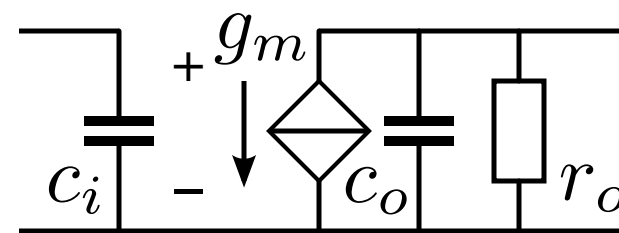
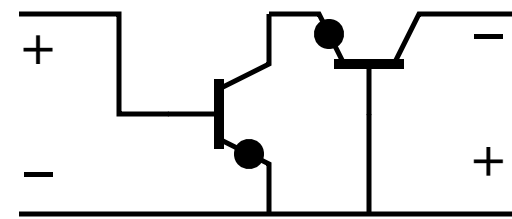
differential pair
cascode stage



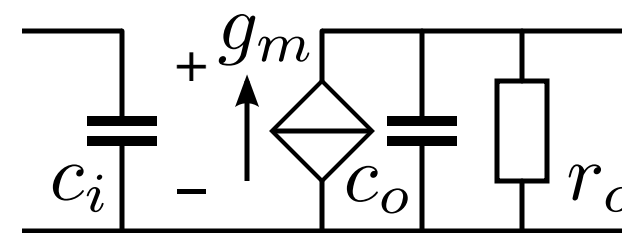
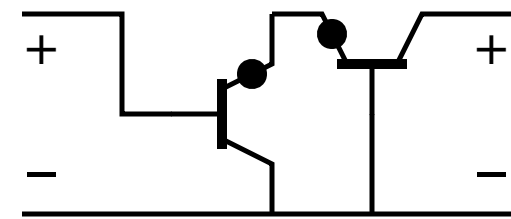
Uni-lateral stages with maximum LP product contribution

Three-terminal

inverting
CS-CG cascode stage

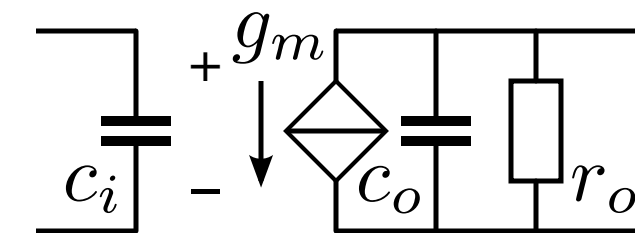
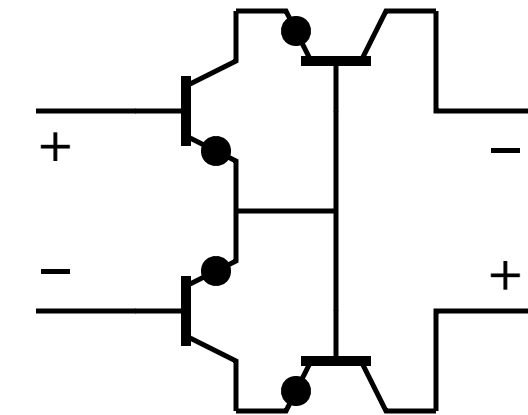


non-inverting
CD-CG cascode stage



Four-terminal

differential pair
cascode stage

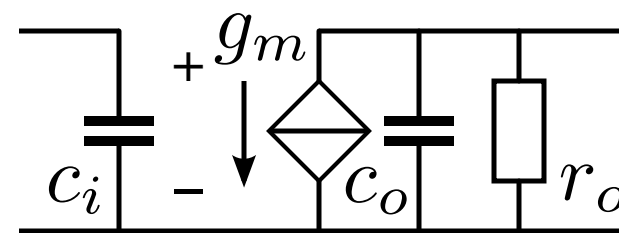
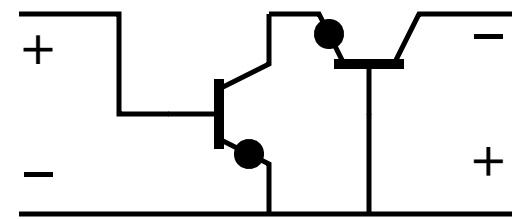


$$g_m = g_{m1}$$

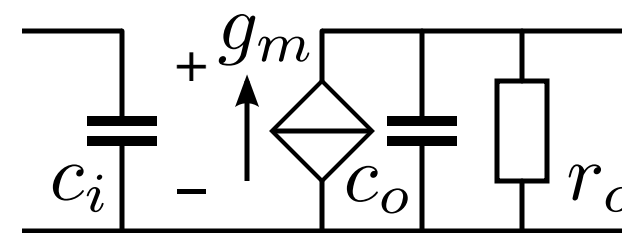
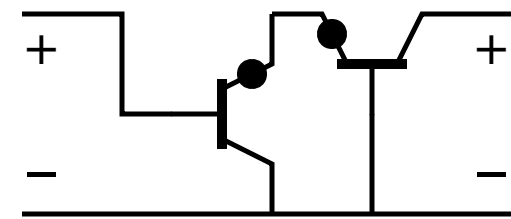
Uni-lateral stages with maximum LP product contribution

Three-terminal

inverting
CS-CG cascode stage

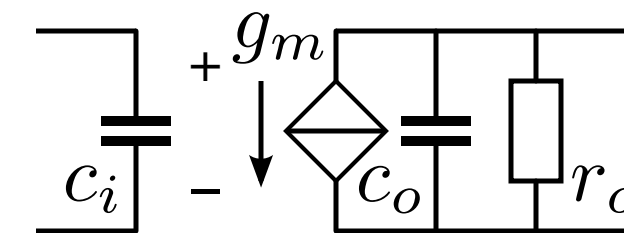
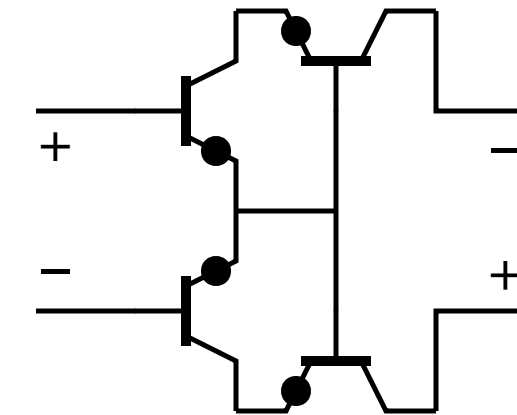


non-inverting
CD-CG cascode stage



Four-terminal

differential pair
cascode stage

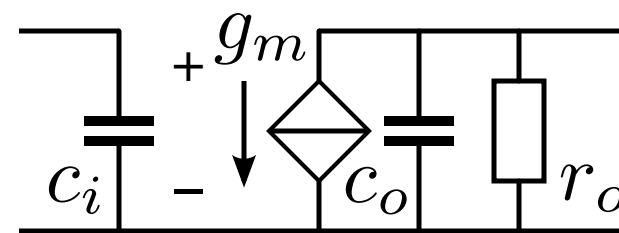
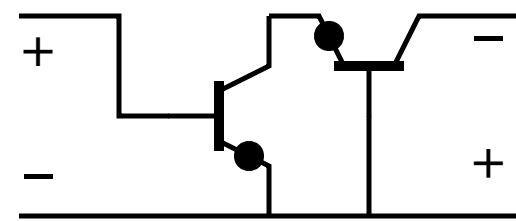


$$g_m = g_{m1} \quad C_i = C_{gs1} + C_{gd1}$$

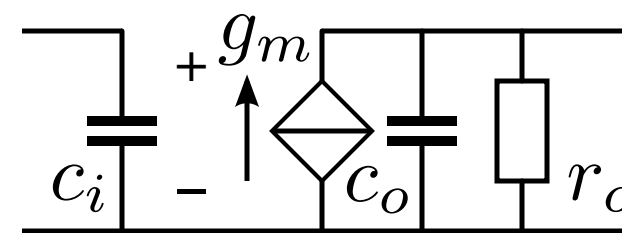
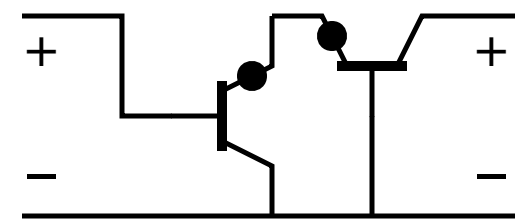
Uni-lateral stages with maximum LP product contribution

Three-terminal

inverting
CS-CG cascode stage

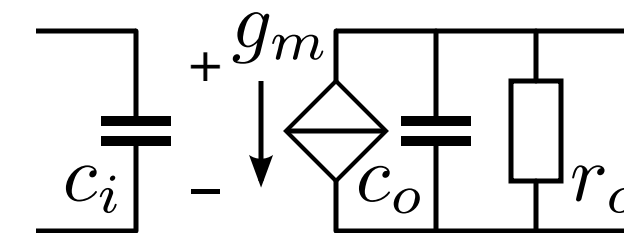
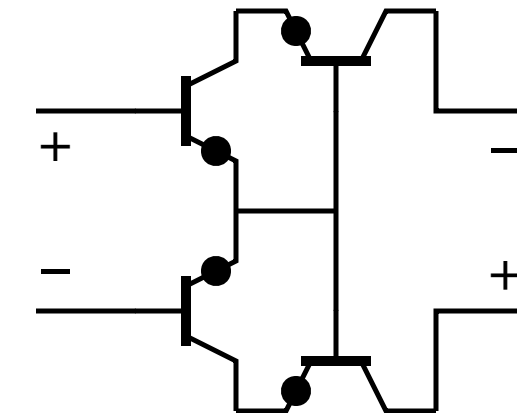


non-inverting
CD-CG cascode stage



Four-terminal

differential pair
cascode stage

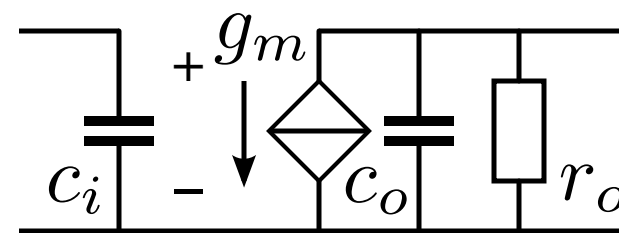
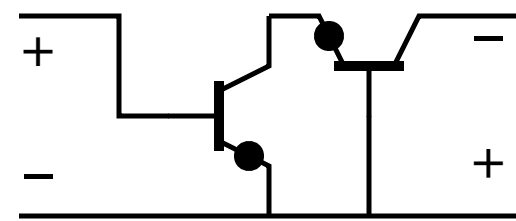


$$g_m = g_{m_1} \quad C_i = C_{gs_1} + C_{gd_1} \quad C_o = C_{gd_2} + C_{db_2}$$

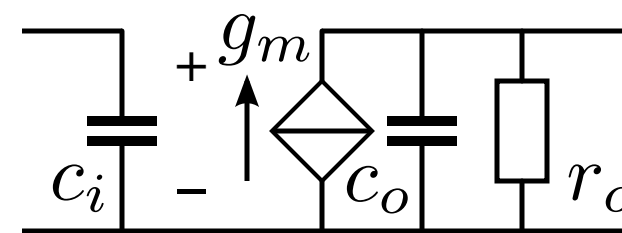
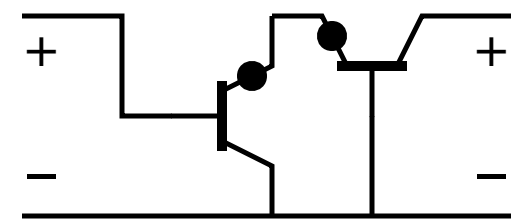
Uni-lateral stages with maximum LP product contribution

Three-terminal

inverting
CS-CG cascode stage

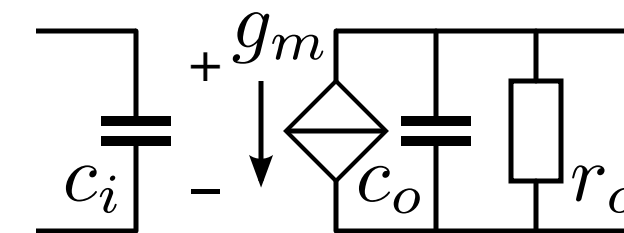
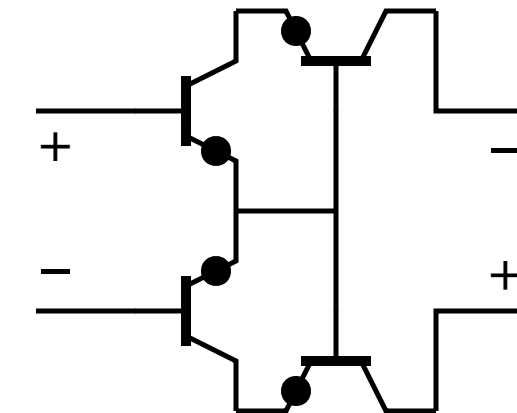


non-inverting
CD-CG cascode stage



Four-terminal

differential pair
cascode stage



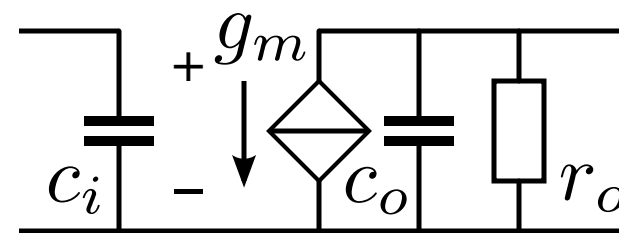
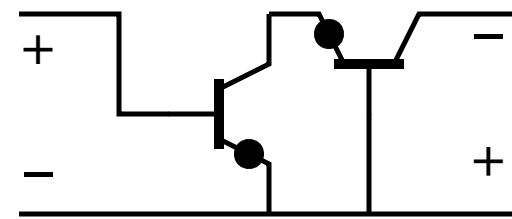
$$g_m = g_{m1} \quad C_i = C_{gs1} + C_{gd1} \quad C_o = C_{gd2} + C_{db2}$$

Current driven:

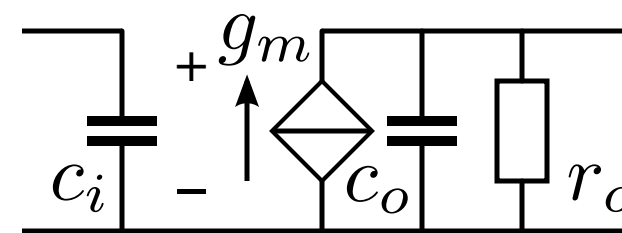
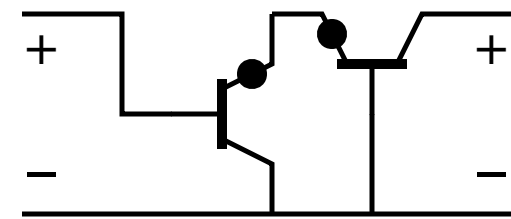
Uni-lateral stages with maximum LP product contribution

Three-terminal

inverting
CS-CG cascode stage

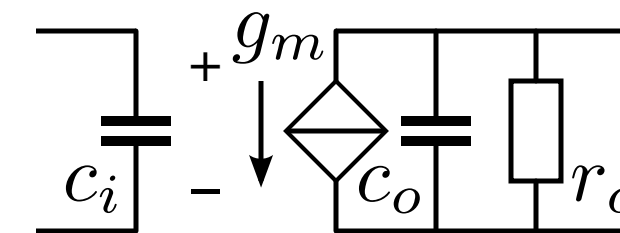
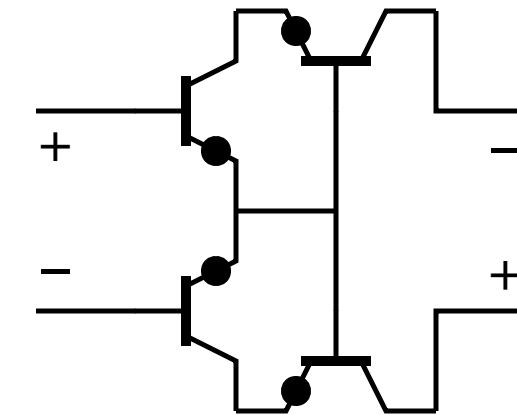


non-inverting
CD-CG cascode stage



Four-terminal

differential pair
cascode stage



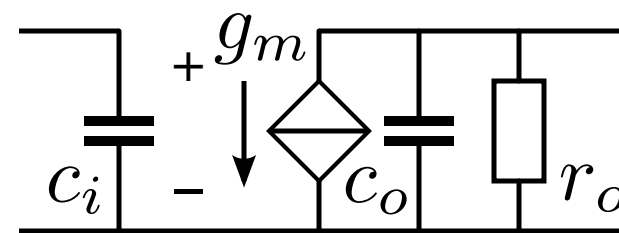
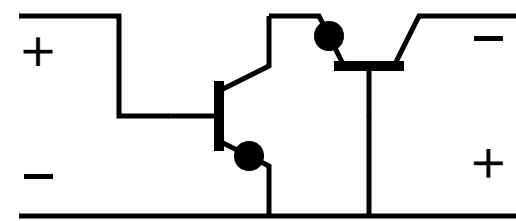
$$g_m = g_{m_1} \quad C_i = C_{gs_1} + C_{gd_1} \quad C_o = C_{gd_2} + C_{db_2}$$

Current driven: $r_o = (1 + g_{m_1} r_{o_1}) r_{o_2}$

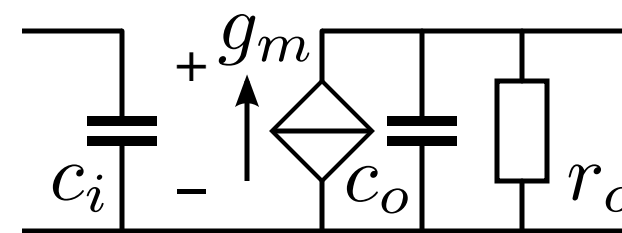
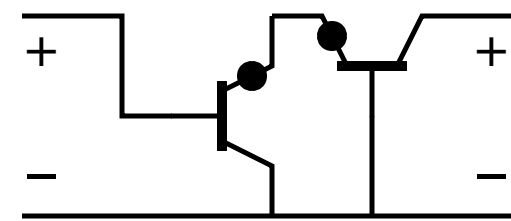
Uni-lateral stages with maximum LP product contribution

Three-terminal

inverting
CS-CG cascode stage

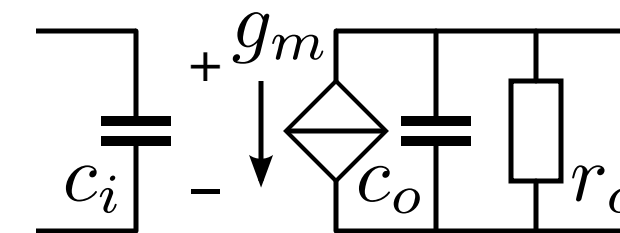
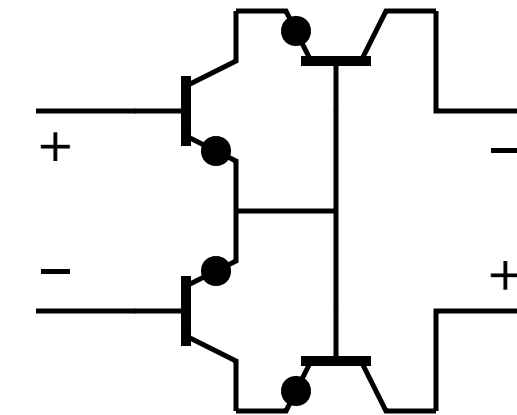


non-inverting
CD-CG cascode stage



Four-terminal

differential pair
cascode stage



$$g_m = g_{m_1} \quad C_i = C_{gs_1} + C_{gd_1} \quad C_o = C_{gd_2} + C_{db_2}$$

$$\text{Current driven: } r_o = (1 + g_{m_1} r_{o_1}) r_{o_2}$$

Number of stages

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Rough estimation based upon required bandwidth:

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LP_1 = single-stage LP product

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m = number of dominant poles of single-stage solution

Number of stages

Rough estimation based upon required bandwidth:

LP_1 = single-stage LP product

f_H = required minimum value of the low-pass cut-off frequency of servo function

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n = minimum number of stages that need to be added to achieve f_H

Number of stages

Rough estimation based upon required bandwidth:

LP_1 = single-stage LP product

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n = minimum number of stages that need to be added to achieve f_H

Design equation:

Number of stages

Rough estimation based upon required bandwidth:

LP_1 = single-stage LP product

f_H = required minimum value of the low-pass cut-off frequency of servo function

m = number of dominant poles of single-stage solution

n = minimum number of stages that need to be added to achieve f_H

Design equation:

$$f_H = \sqrt[n+m]{f_T^n LP_1}$$

Number of stages

Rough estimation based upon required bandwidth:

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m = number of dominant poles of single-stage solution

n = minimum number of stages that need to be added to achieve f_H

Design equation:

Solution:

$$f_H = \sqrt[n+m]{f_T^n LP_1}$$

Number of stages

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LP_1 = single-stage LP product

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Design equation:

$$f_H = \sqrt[n+m]{f_T^n LP_1}$$

Solution:

$$n = \frac{m \log f_H - \log LP_1}{\log \frac{f_T}{f_H}}$$

Number of stages

Rough estimation based upon required bandwidth:

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What if the bandwidth is large enough and the number of stages is based upon the VI drive capability or the weak distortion?

Number of stages

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What if the bandwidth is large enough and the number of stages is based upon the VI drive capability or the weak distortion?

IF: Frequency compensation necessary and possible
(without adversely affecting drive capability and distortion):

Number of stages

Rough estimation based upon required bandwidth:

LP_1 = single-stage LP product

f_H = required minimum value of the low-pass cut-off frequency of servo function

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n = minimum number of stages that need to be added to achieve f_H

Design equation:

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What if the bandwidth is large enough and the number of stages is based upon the VI drive capability or the weak distortion?

IF: Frequency compensation necessary and possible
(without adversely affecting drive capability and distortion):

THEN:

Number of stages

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LP_1 = single-stage LP product

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What if the bandwidth is large enough and the number of stages is based upon the VI drive capability or the weak distortion?

IF: Frequency compensation necessary and possible
(without adversely affecting drive capability and distortion):

THEN: **Do frequency compensation**

Number of stages

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What if the bandwidth is large enough and the number of stages is based upon the VI drive capability or the weak distortion?

IF: Frequency compensation necessary and possible
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THEN: Do frequency compensation

ELSE:

Number of stages

Rough estimation based upon required bandwidth:

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What if the bandwidth is large enough and the number of stages is based upon the VI drive capability or the weak distortion?

IF: Frequency compensation necessary and possible
(without adversely affecting drive capability and distortion):

THEN: Do frequency compensation

ELSE: [Design cascade connection of two amplifiers](#)

Number of stages

Rough estimation based upon required bandwidth:

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What if the bandwidth is large enough and the number of stages is based upon the VI drive capability or the weak distortion?

IF: Frequency compensation necessary and possible
(without adversely affecting drive capability and distortion):

THEN: Do frequency compensation

ELSE: Design cascade connection of two amplifiers

Structured Electronic Design

EE4109

Controller design:
Interconnection of stages

Anton J.M. Montagne

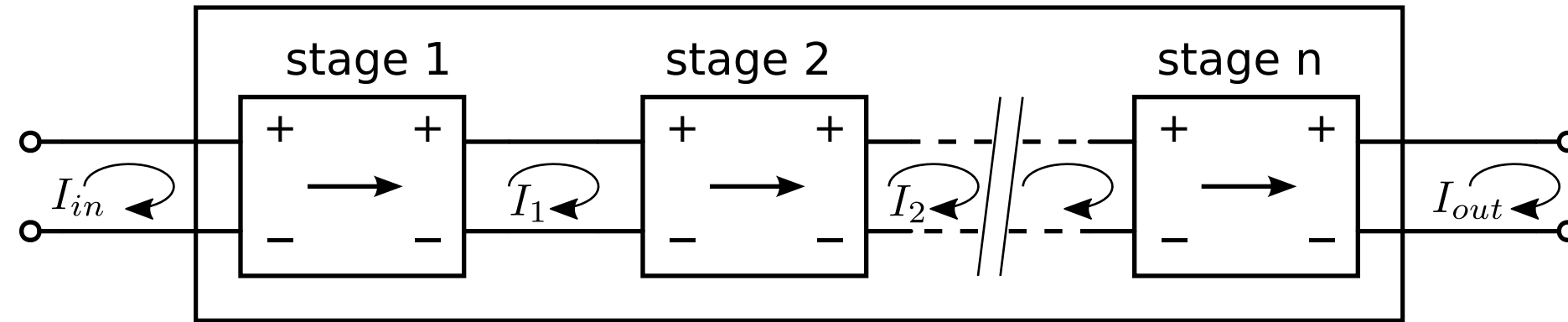
Interconnection of stages

Interconnection of stages

Proper cascade connection

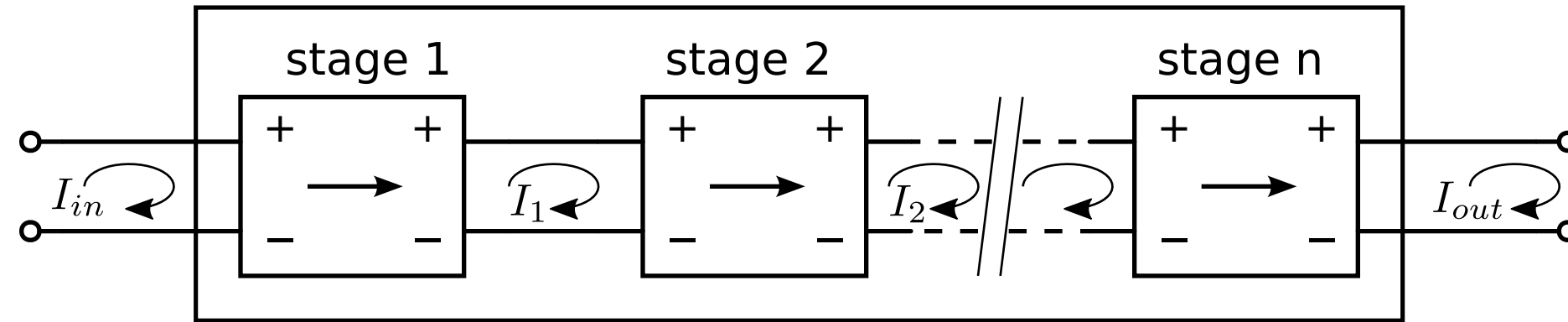
Interconnection of stages

Proper cascade connection



Interconnection of stages

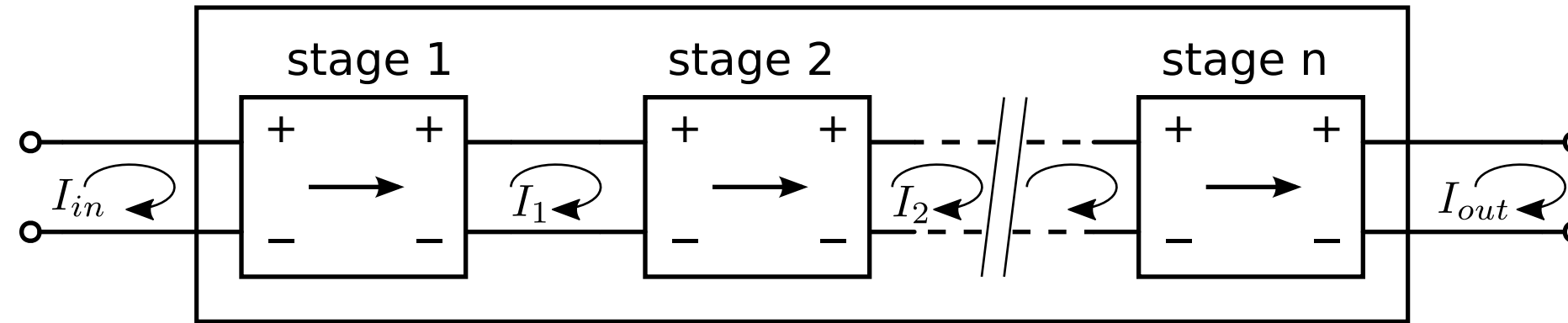
Proper cascade connection



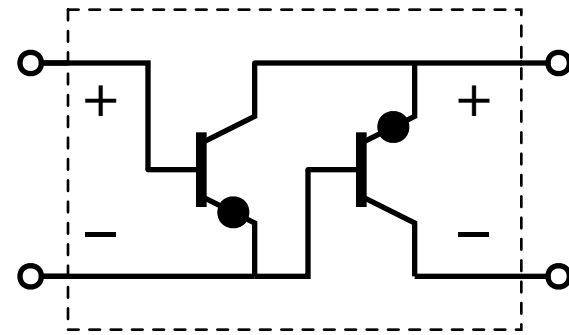
Examples two-stage controllers

Interconnection of stages

Proper cascade connection

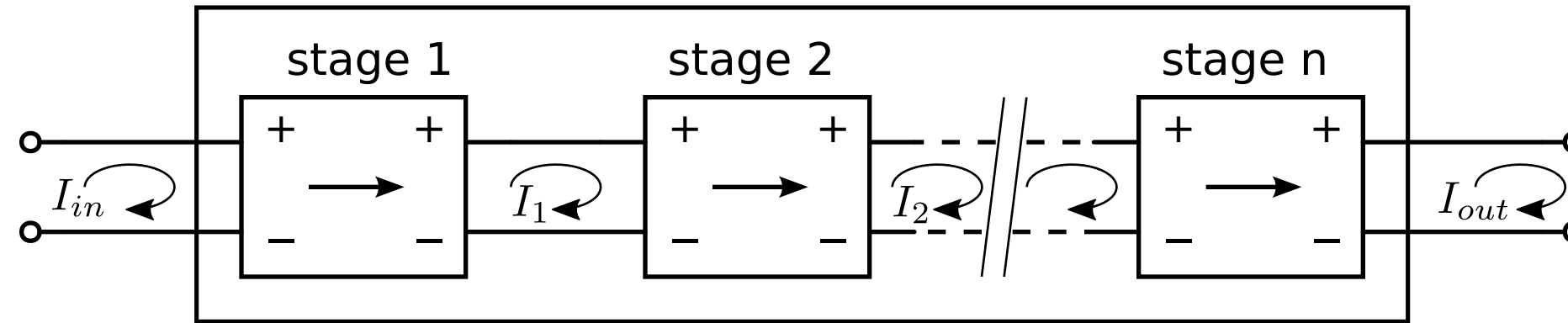


Examples two-stage controllers

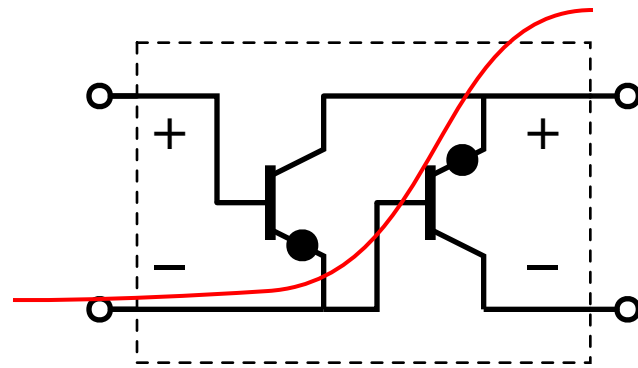


Interconnection of stages

Proper cascade connection



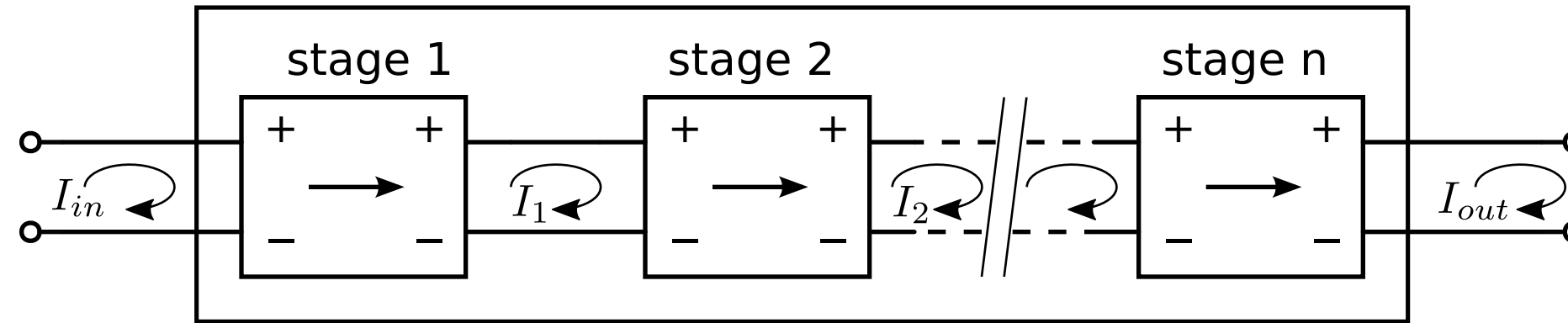
Examples two-stage controllers



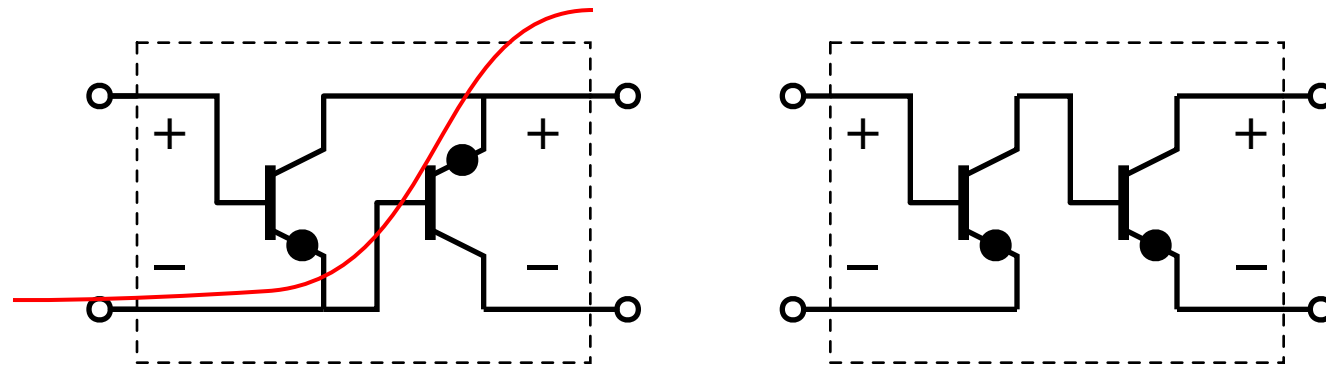
No port isolation.
Can only be used in combination
with a transformer connected to
one of the ports.

Interconnection of stages

Proper cascade connection



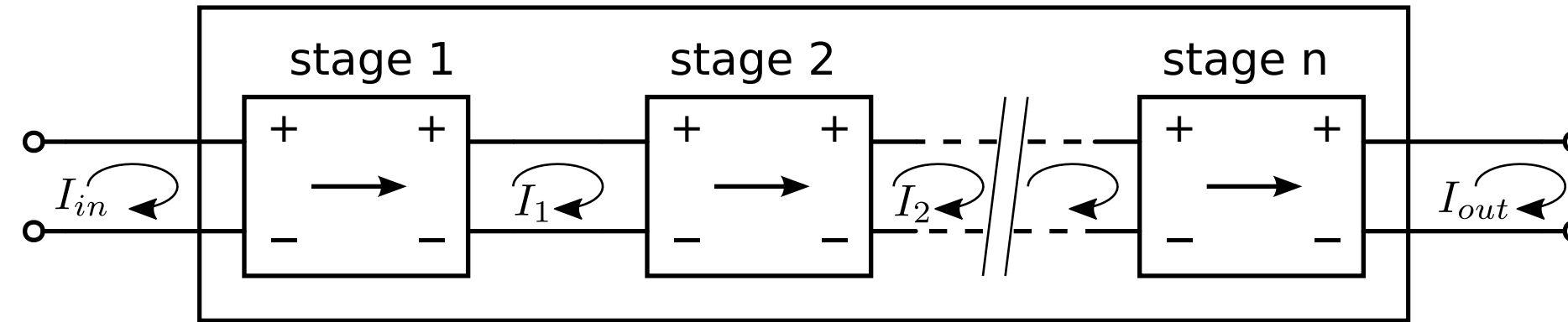
Examples two-stage controllers



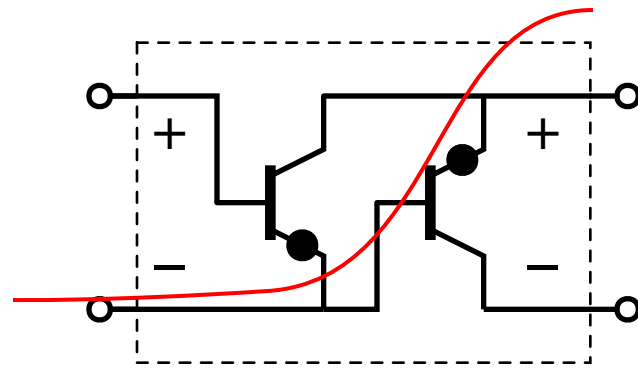
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Interconnection of stages

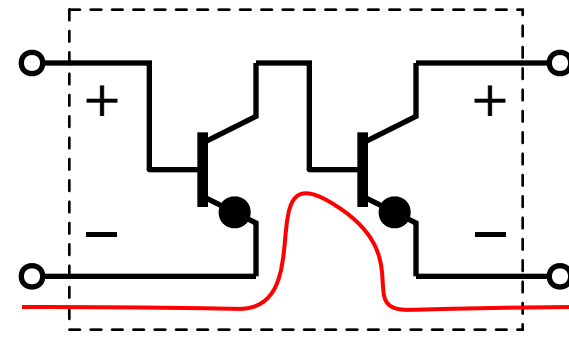
Proper cascade connection



Examples two-stage controllers



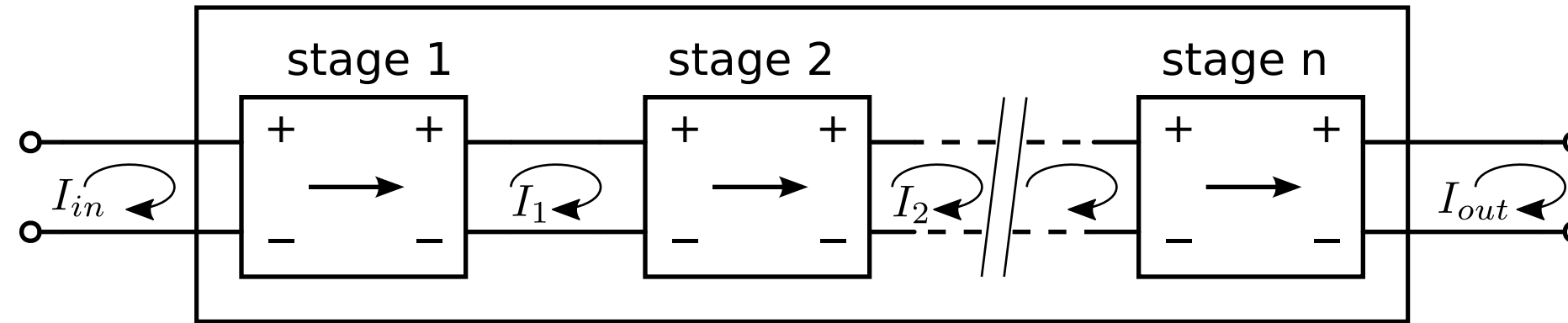
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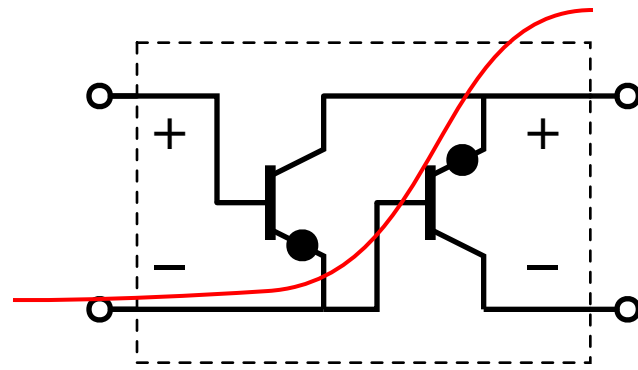
Simple two-transistor controller.
Input current of the second
stage flows through the
external network.

Interconnection of stages

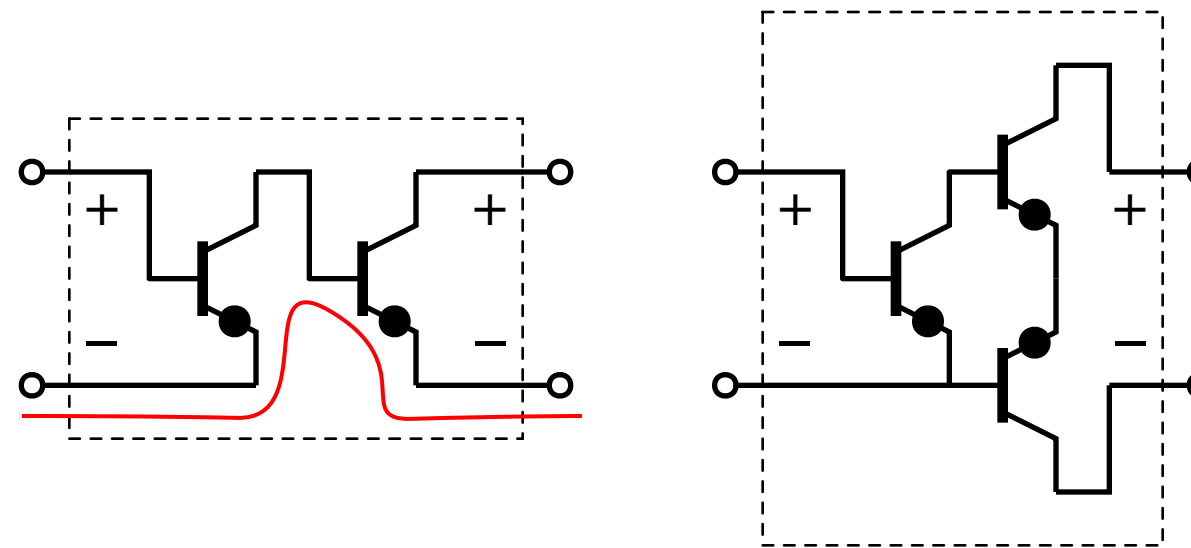
Proper cascade connection



Examples two-stage controllers



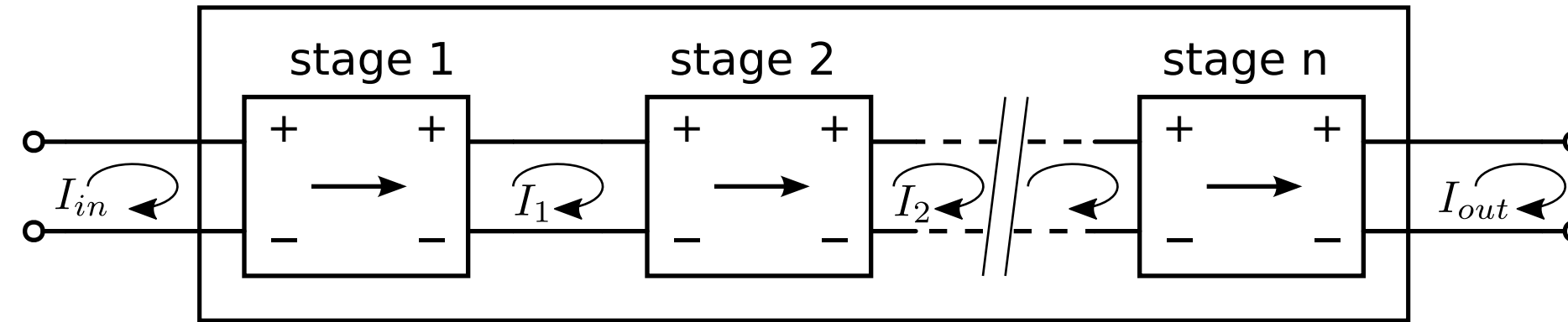
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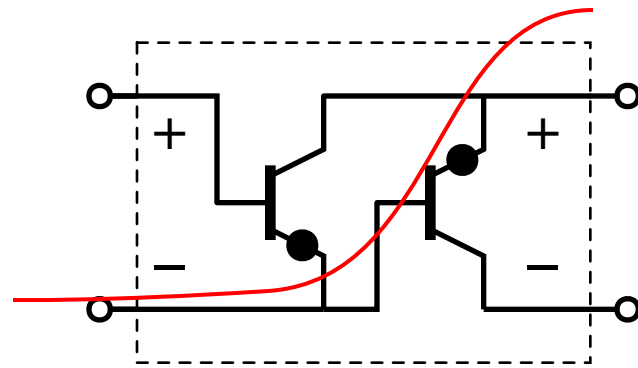
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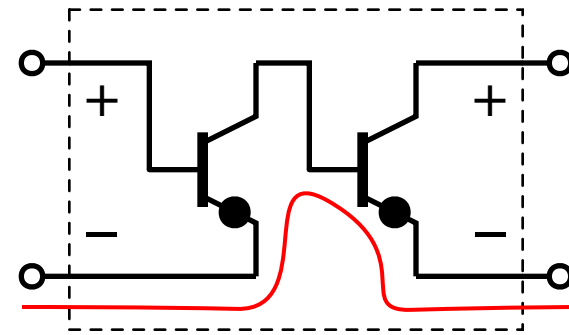
Proper cascade connection



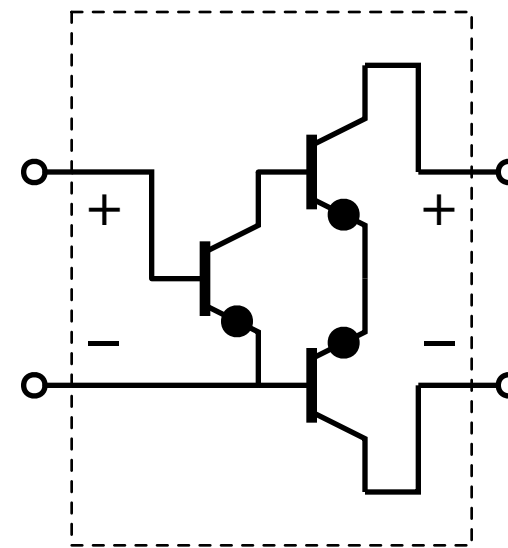
Examples two-stage controllers



No port isolation.
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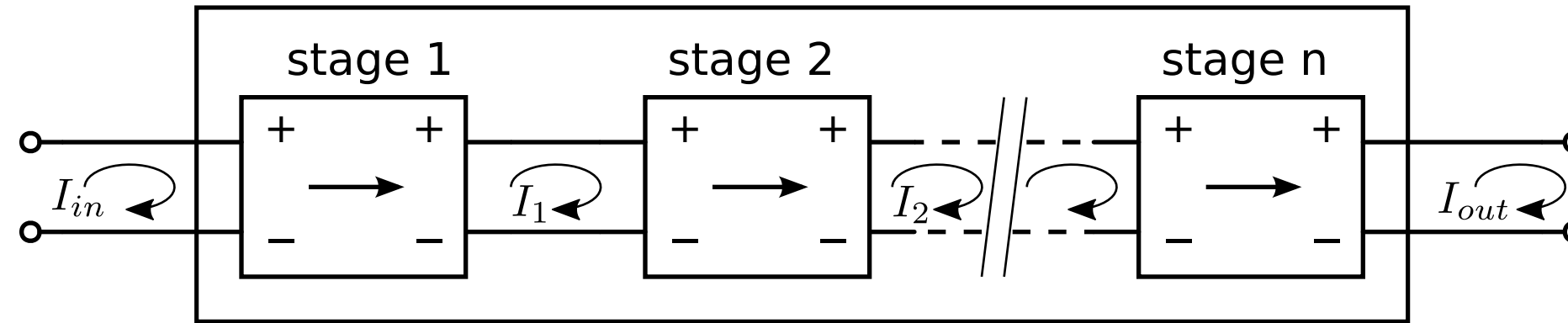
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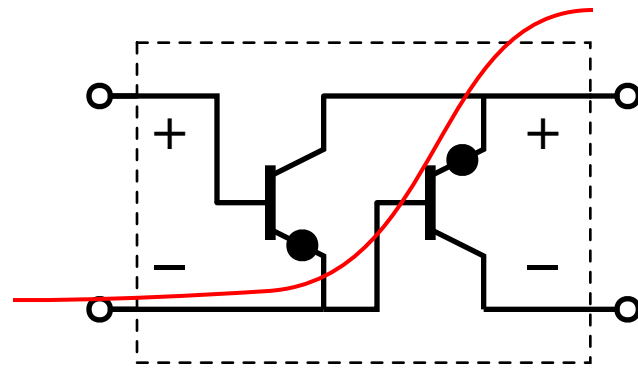
Two-stage controller with
anti-series output stage.

Interconnection of stages

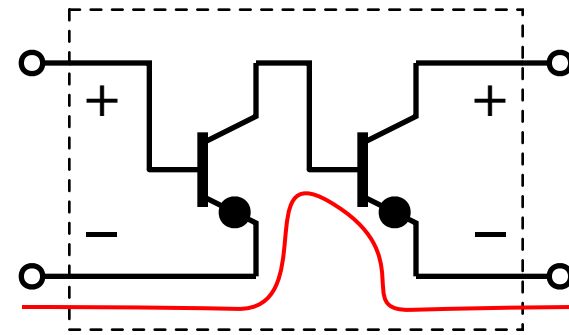
Proper cascade connection



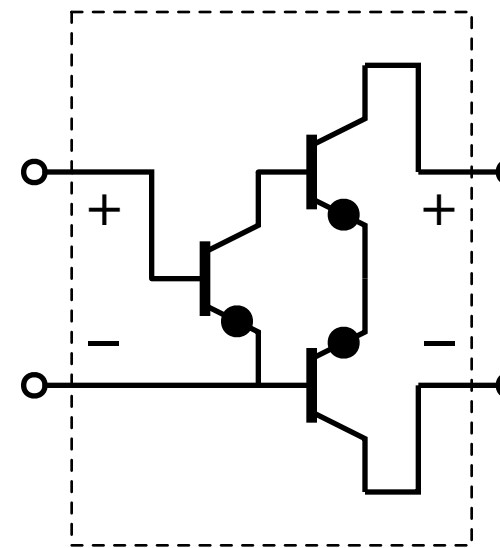
Examples two-stage controllers



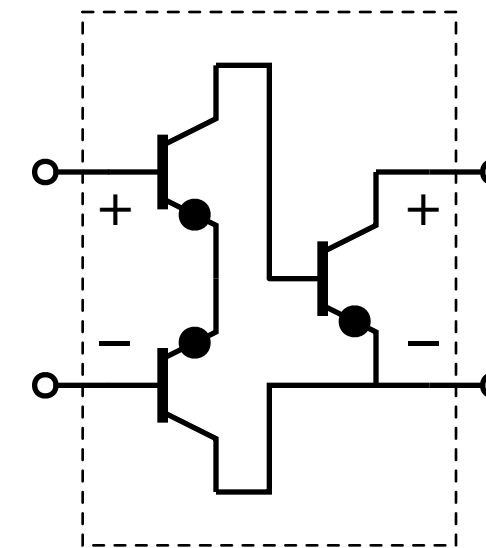
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Simple two-transistor controller.
Input current of the second
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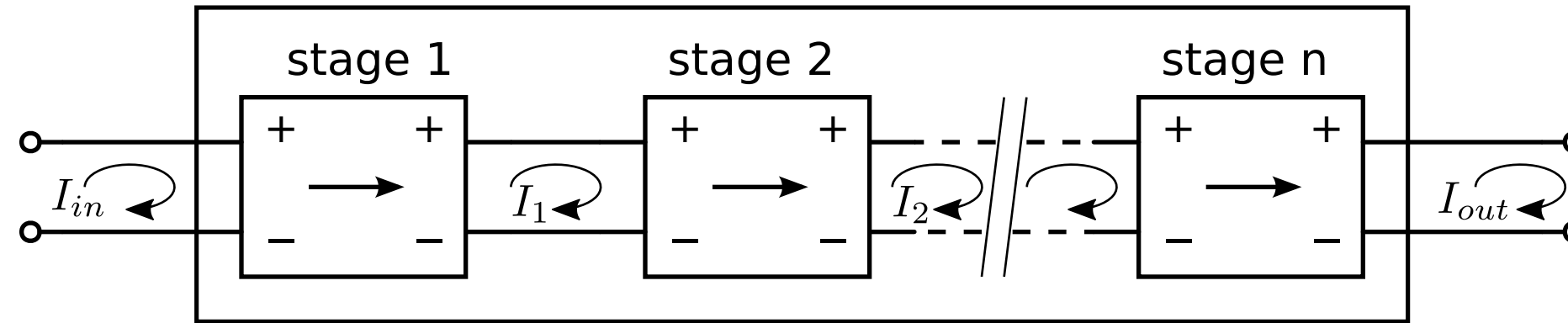


Two-stage controller with
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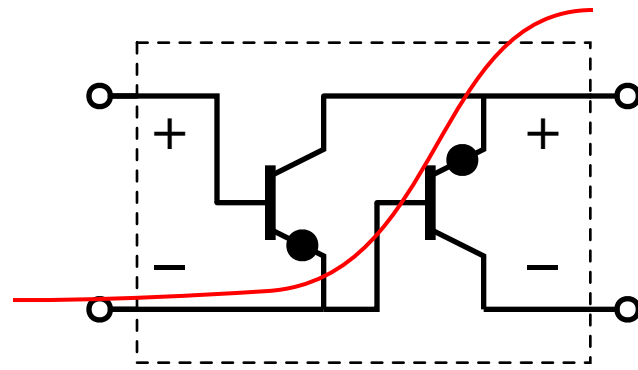


Interconnection of stages

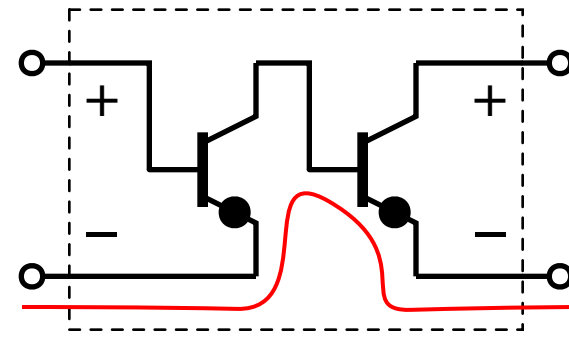
Proper cascade connection



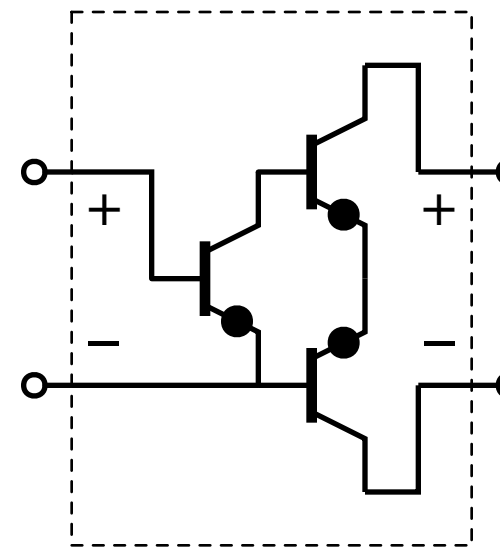
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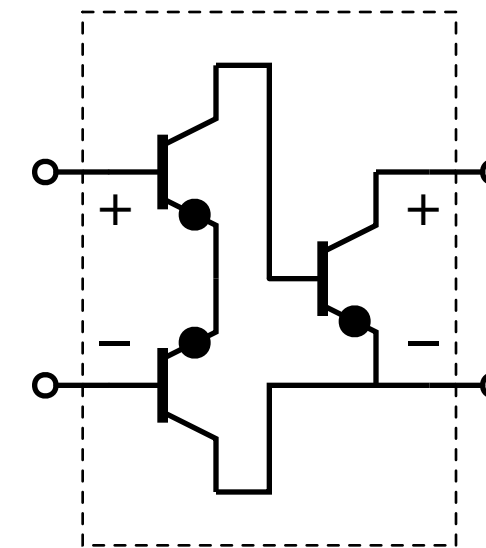
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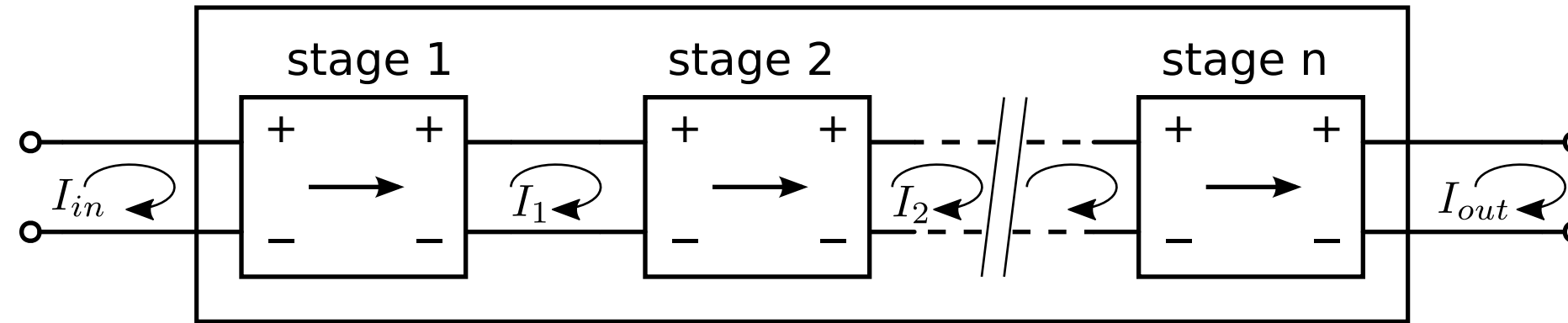
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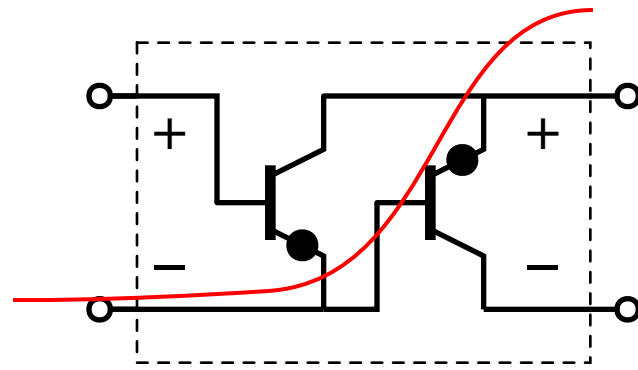
Two-stage controller with
anti-series input stage.
A push-pull stage can be
used for the second stage.

Interconnection of stages

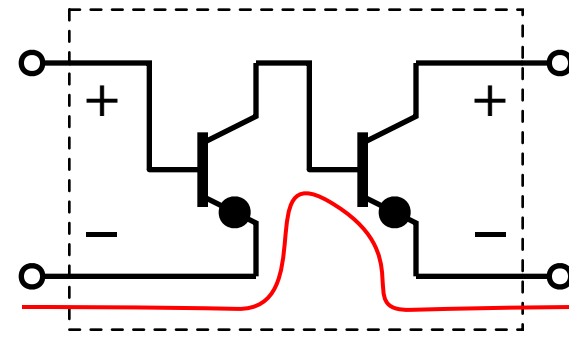
Proper cascade connection



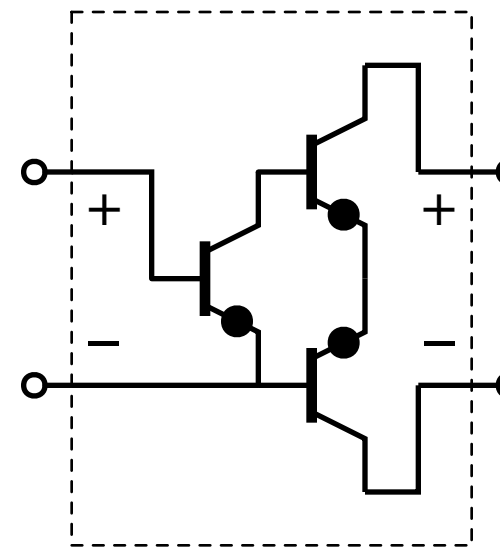
Examples two-stage controllers



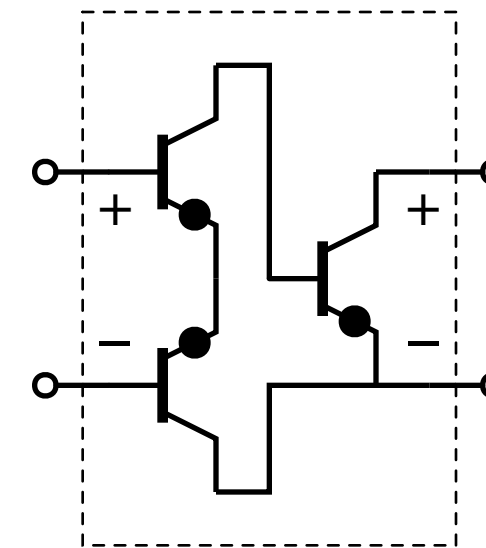
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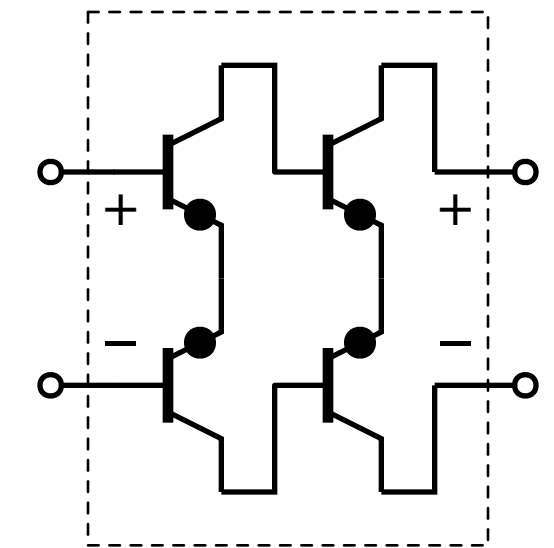
Simple two-transistor controller.
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Two-stage controller with
anti-series output stage.

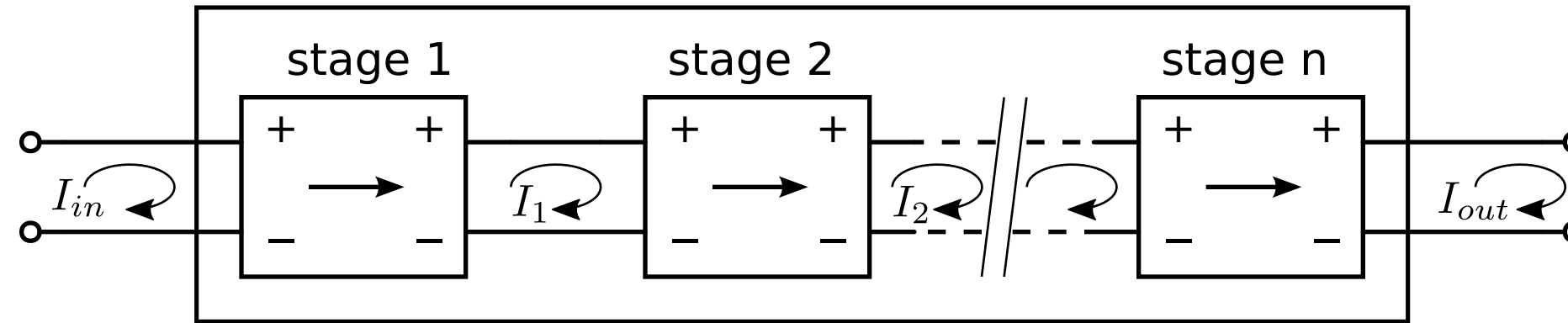


Two-stage controller with
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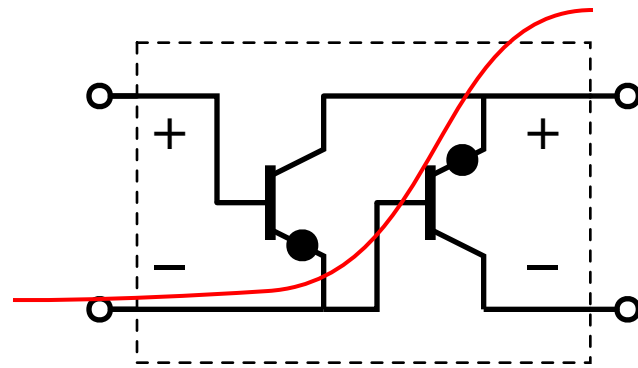


Interconnection of stages

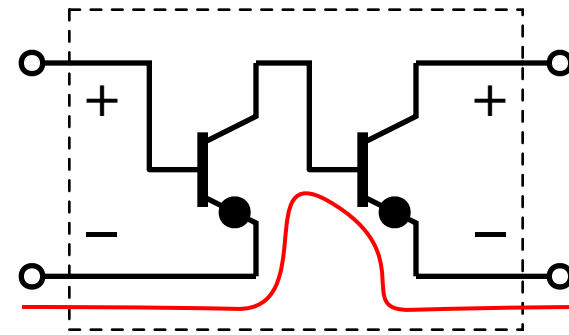
Proper cascade connection



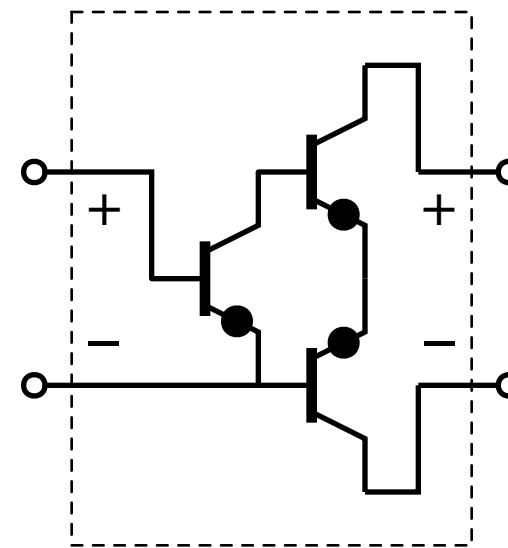
Examples two-stage controllers



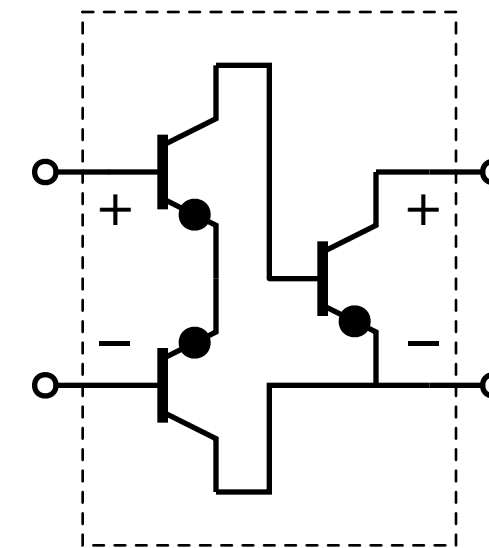
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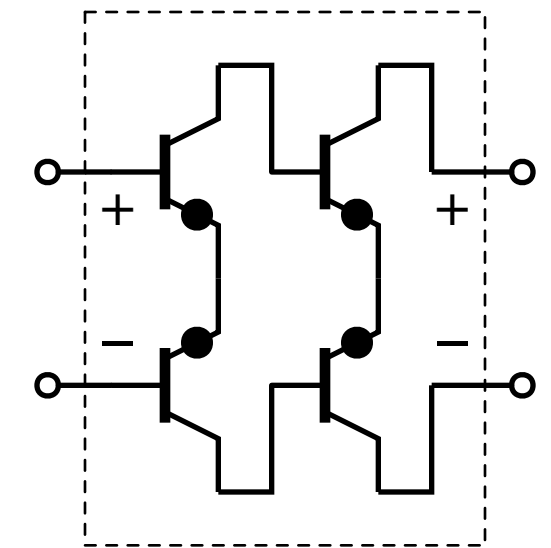
Simple two-transistor controller.
Input current of the second
stage flows through the
external network.



Two-stage controller with
anti-series output stage.



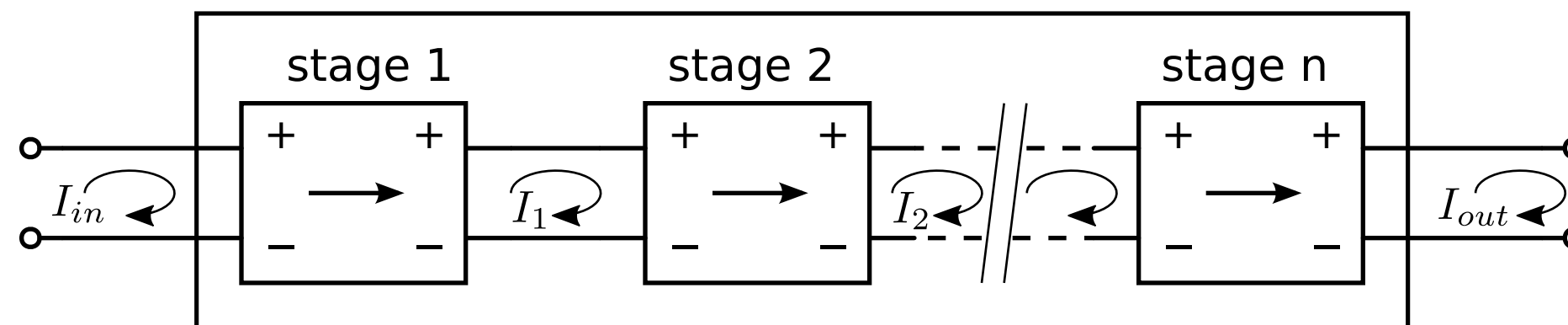
Two-stage controller with
anti-series input stage.
A push-pull stage can be
used for the second stage.



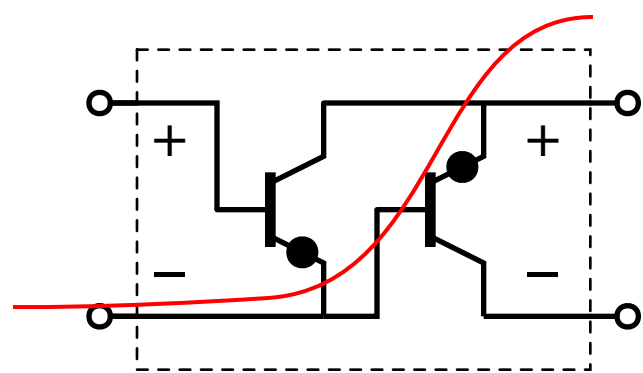
Fully balanced two-stage
controller.

Interconnection of stages

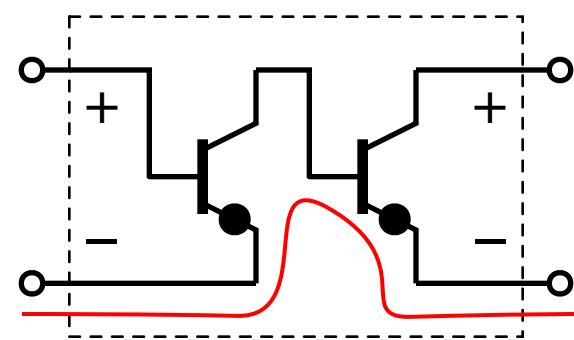
Proper cascade connection



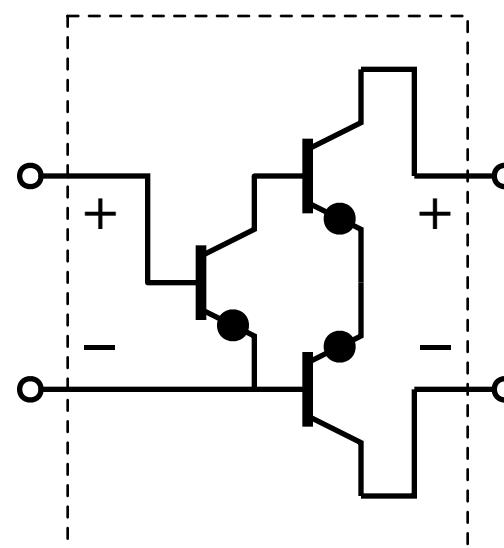
Examples two-stage controllers



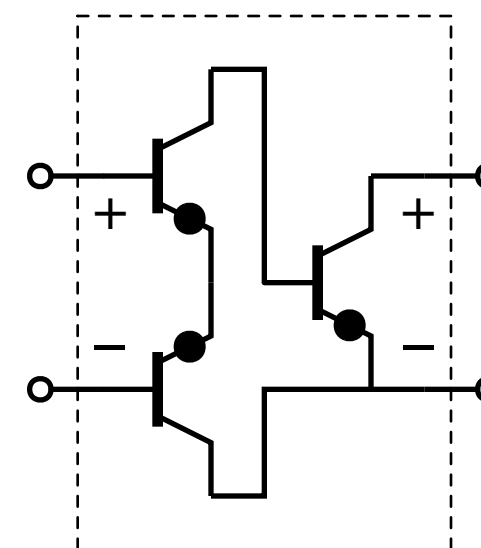
No port isolation.
Can only be used in combination
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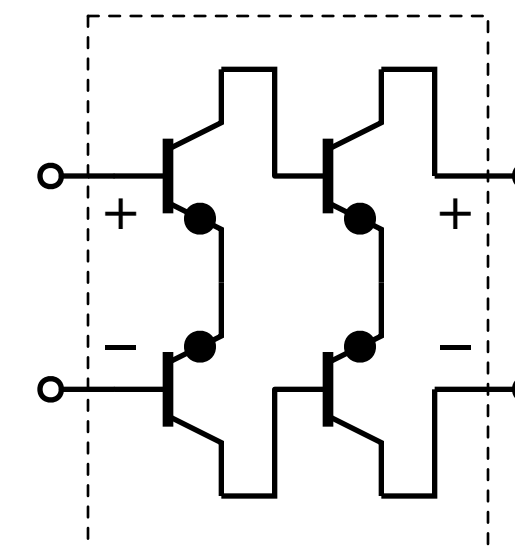
Simple two-transistor controller.
Input current of the second
stage flows through the
external network.



Two-stage controller with
anti-series output stage.



Two-stage controller with
anti-series input stage.
A push-pull stage can be
used for the second stage.



Fully balanced two-stage
controller.

Interconnection of stages

Interconnection of stages

Four terminal controller options

Interconnection of stages

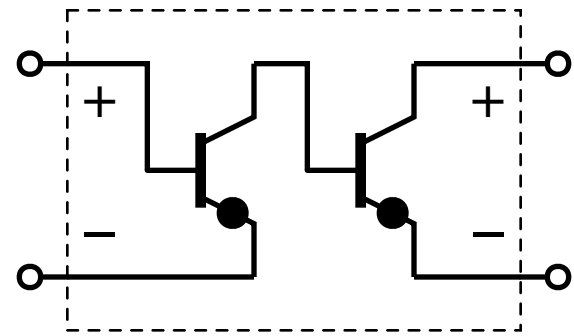
Four terminal controller options

Reverse connections of both
the input port and the output port

Interconnection of stages

Four terminal controller options

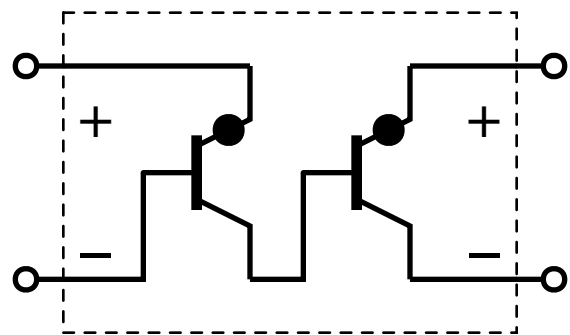
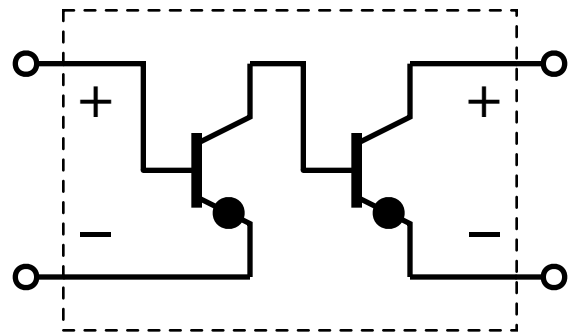
Reverse connections of both
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Interconnection of stages

Four terminal controller options

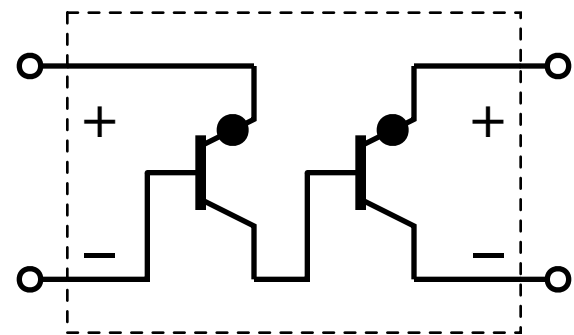
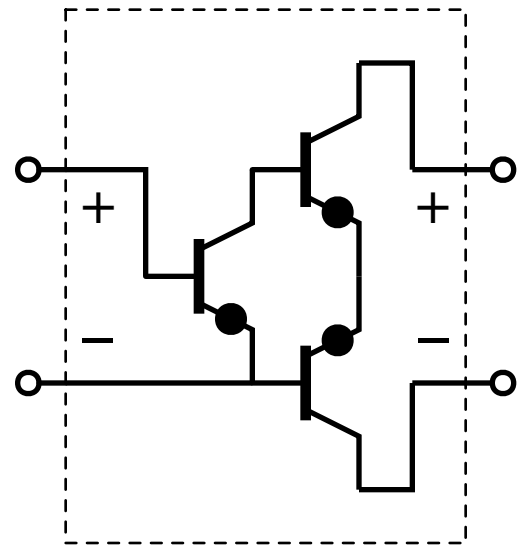
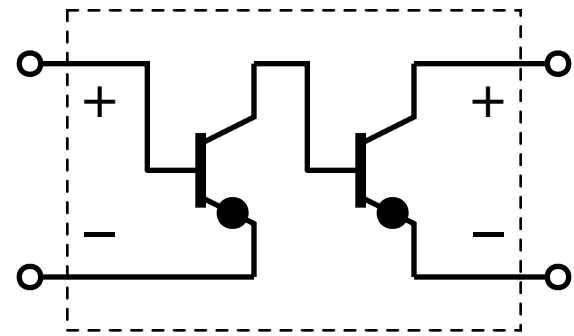
Reverse connections of both
the input port and the output port



Interconnection of stages

Four terminal controller options

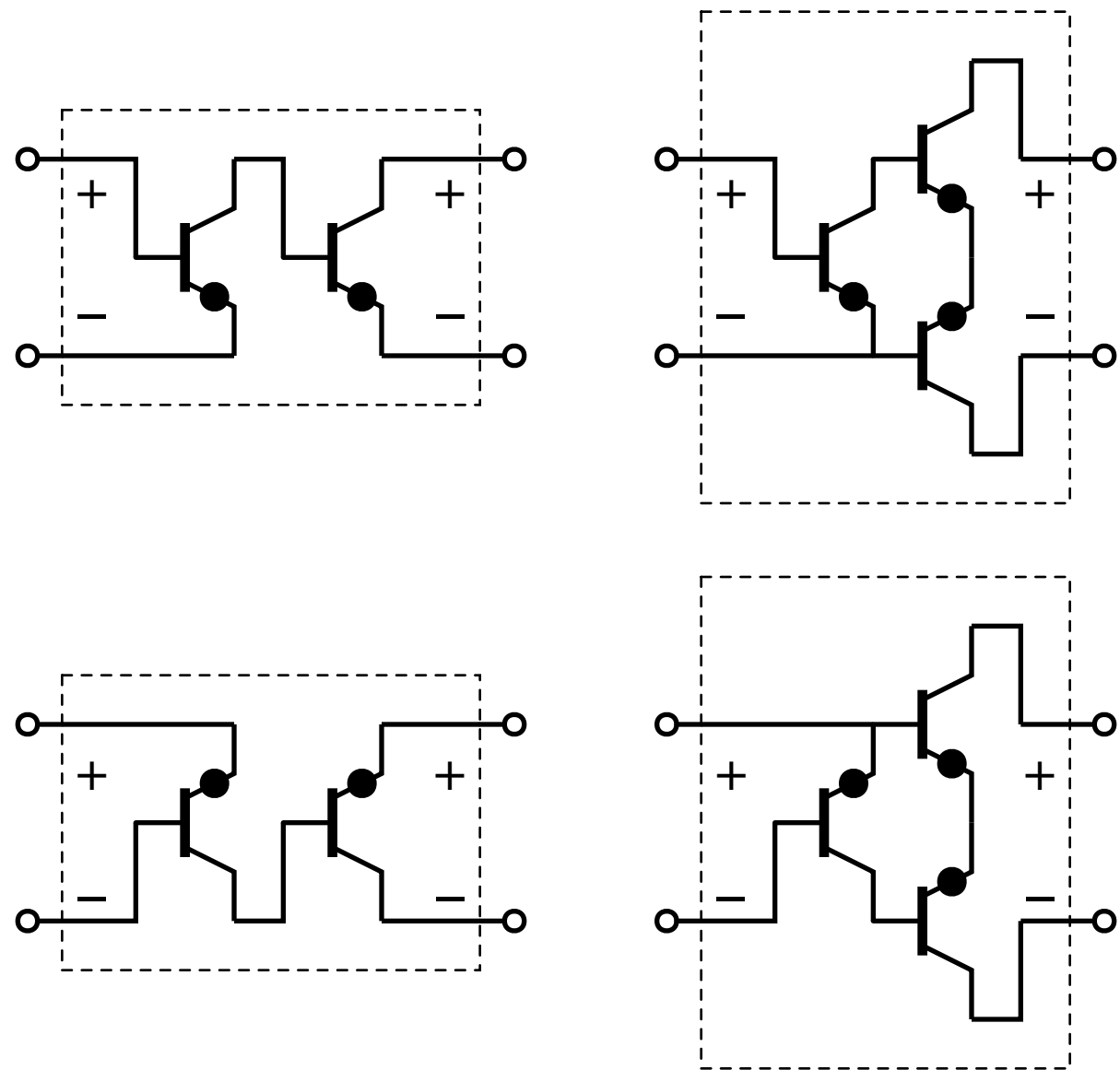
Reverse connections of both
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Interconnection of stages

Four terminal controller options

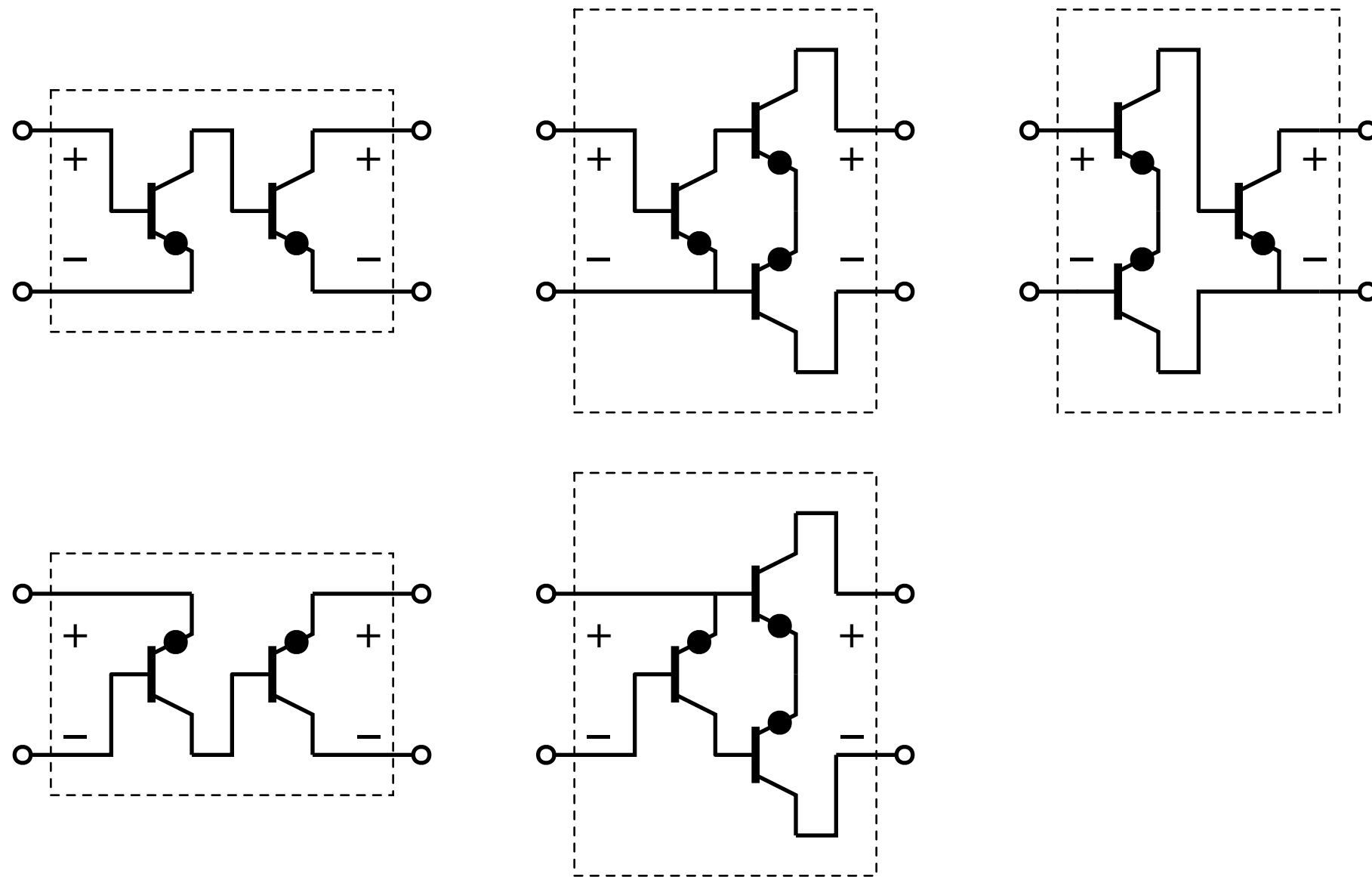
Reverse connections of both
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Interconnection of stages

Four terminal controller options

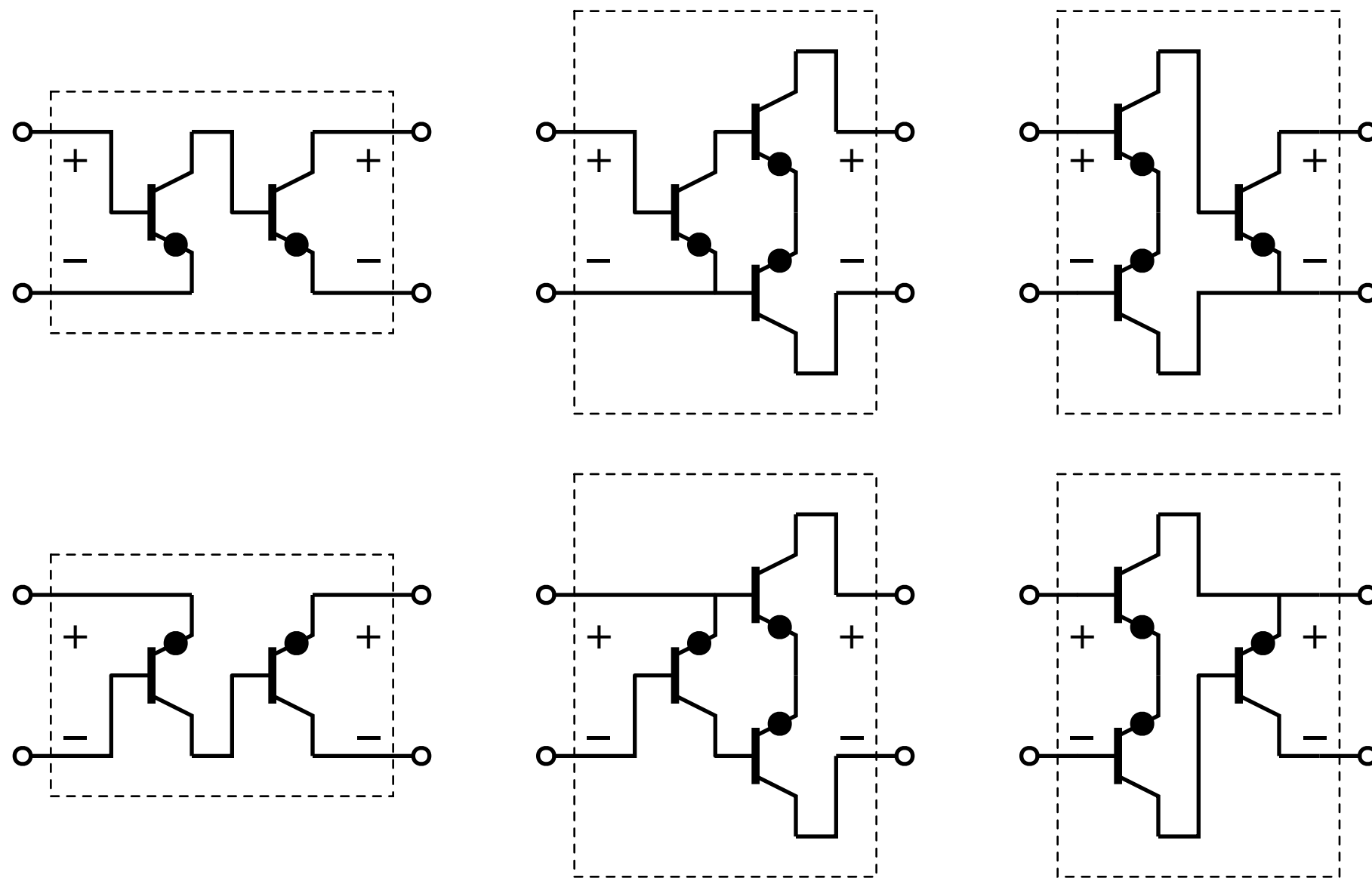
Reverse connections of both
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Interconnection of stages

Four terminal controller options

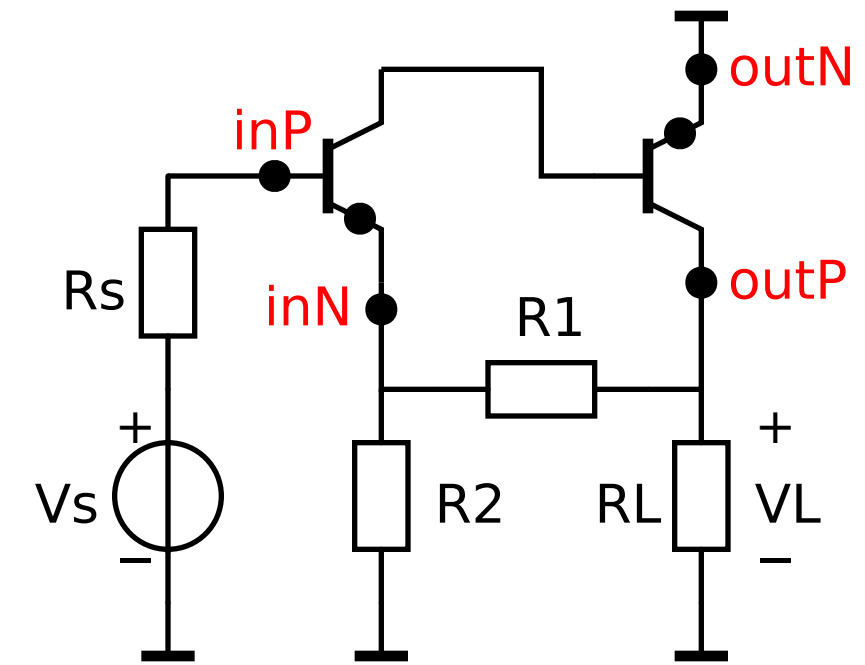
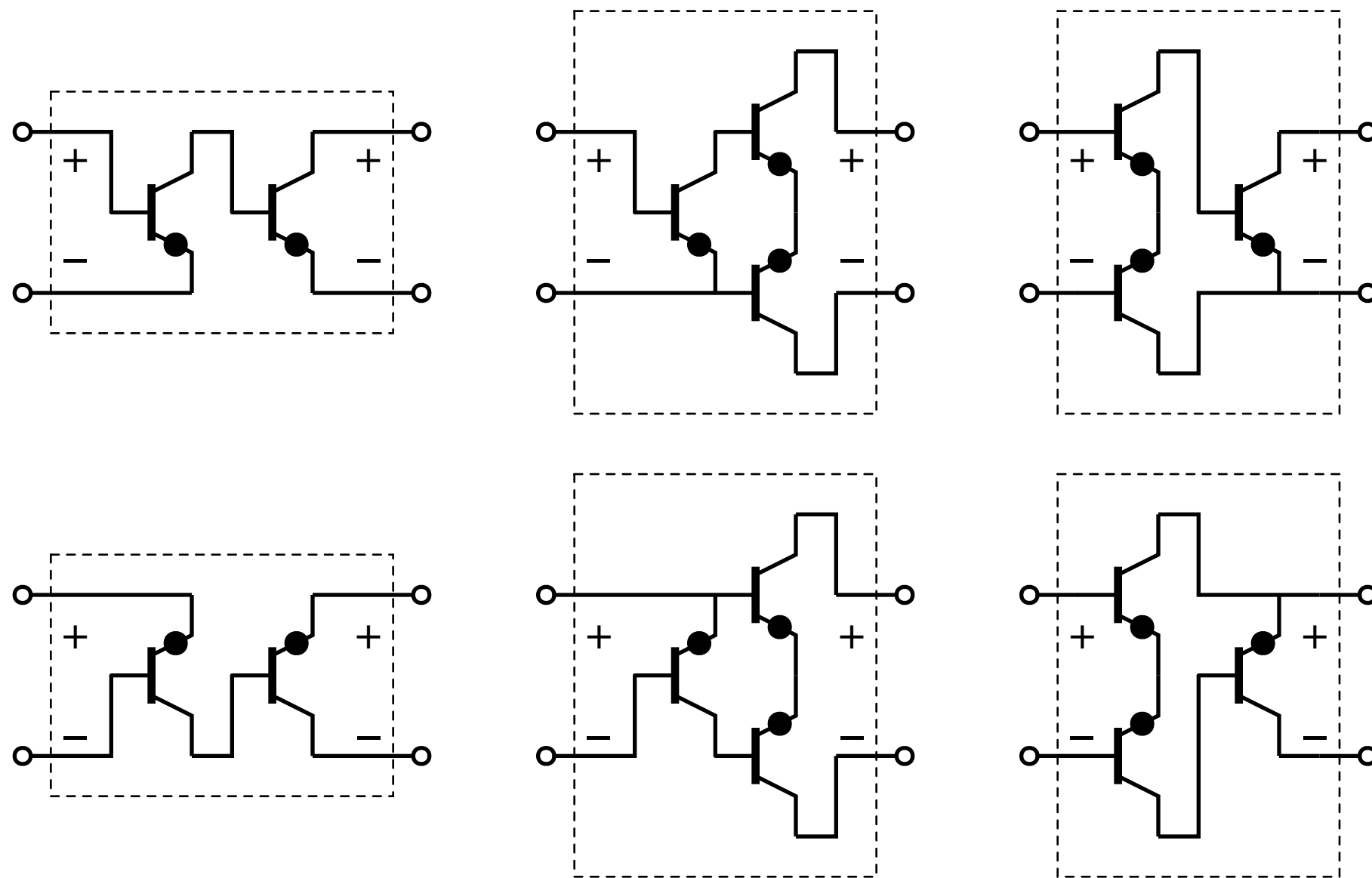
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Interconnection of stages

Four terminal controller options

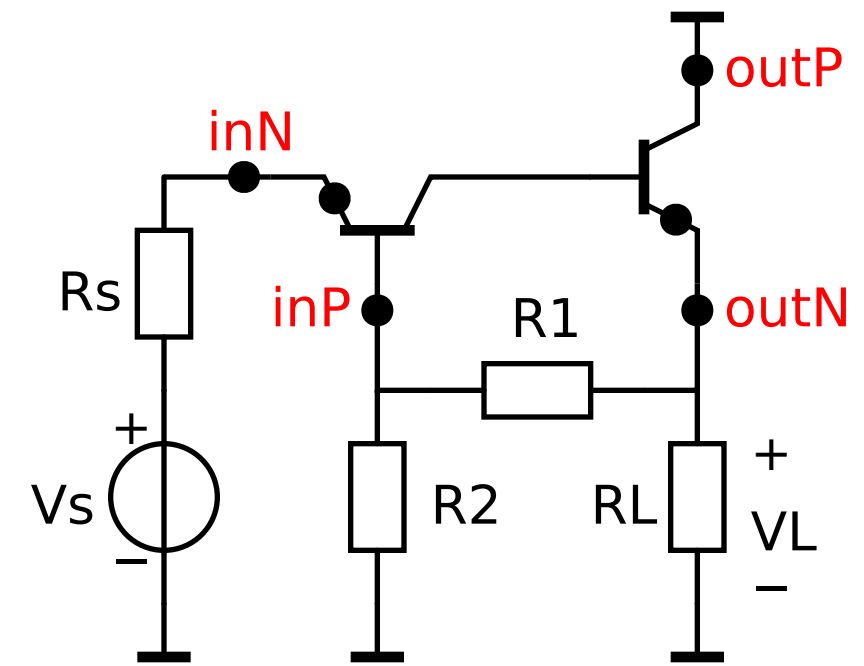
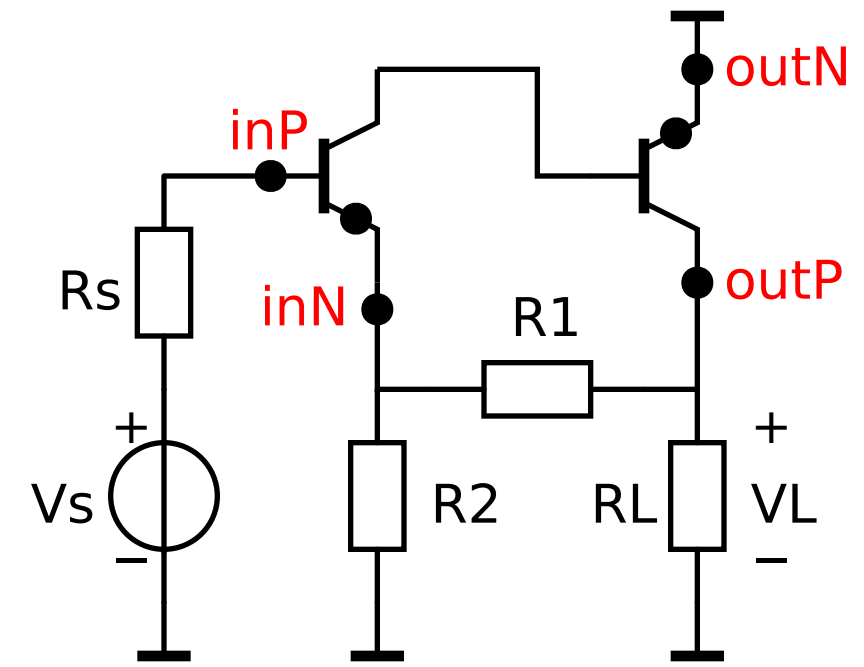
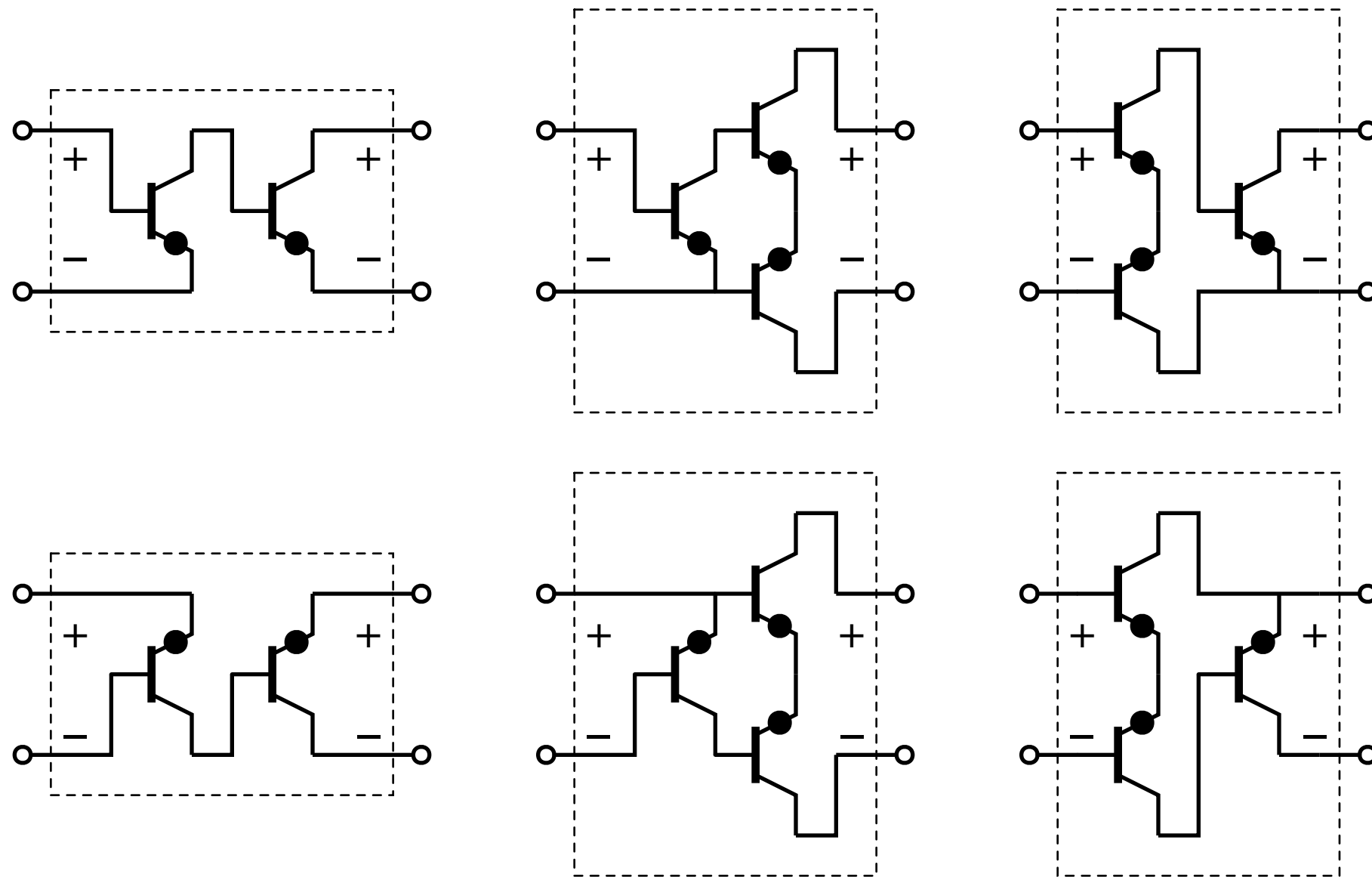
Reverse connections of both the input port and the output port



Interconnection of stages

Four terminal controller options

Reverse connections of both the input port and the output port



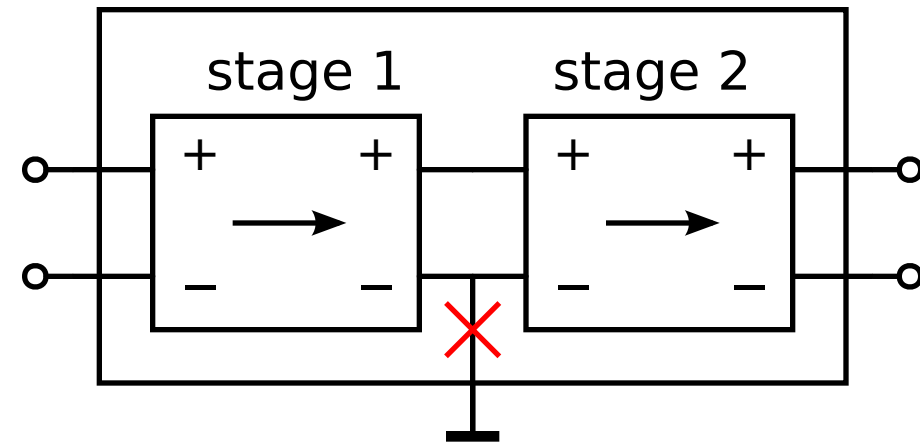
Interconnection of stages

Interconnection of stages

Port isolation considerations

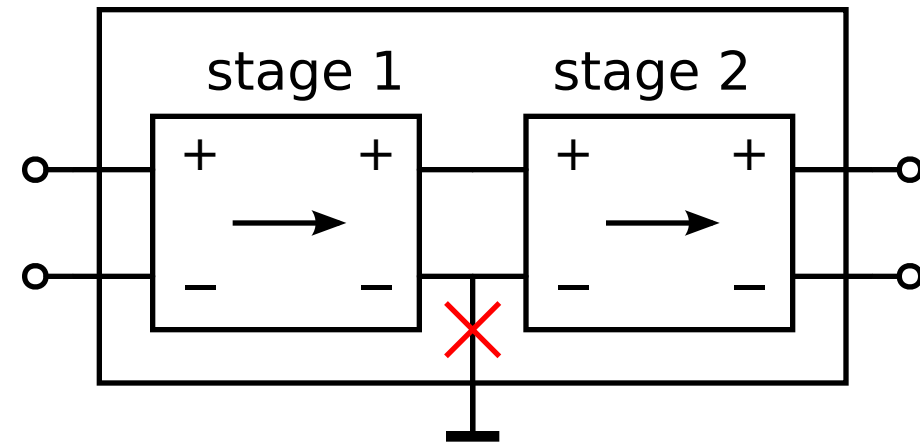
Interconnection of stages

Port isolation considerations



Interconnection of stages

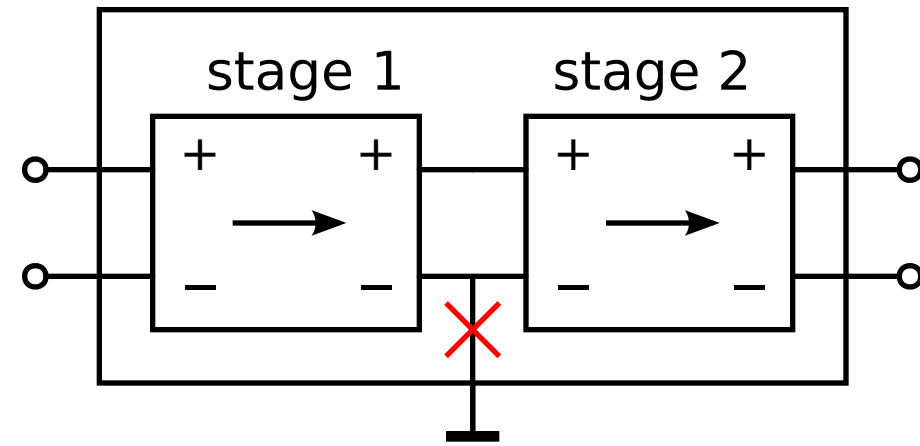
Port isolation considerations



Internal ground connection:

Interconnection of stages

Port isolation considerations

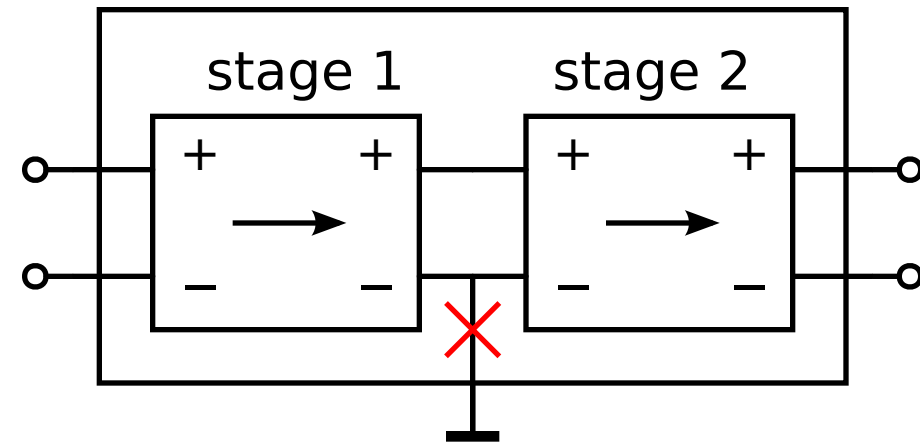


Internal ground connection:

Two-port conditions no longer valid.

Interconnection of stages

Port isolation considerations



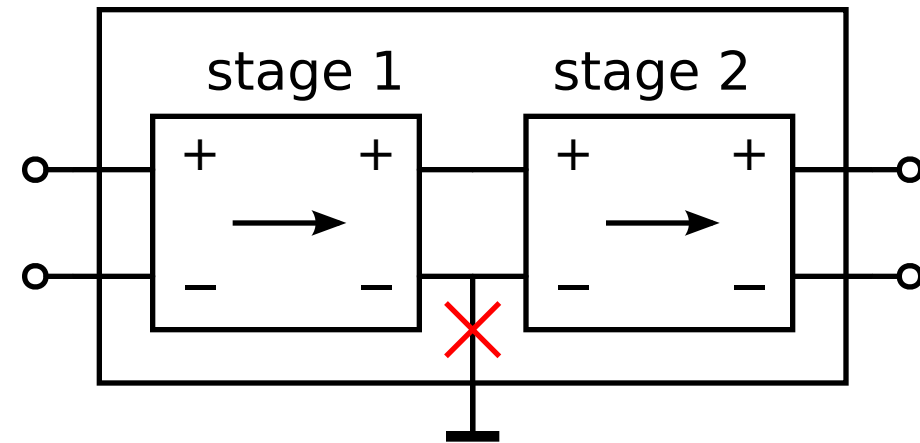
Internal ground connection:

Two-port conditions no longer valid.

Ideal gain may differ from asymptotic gain

Interconnection of stages

Port isolation considerations



Internal ground connection:

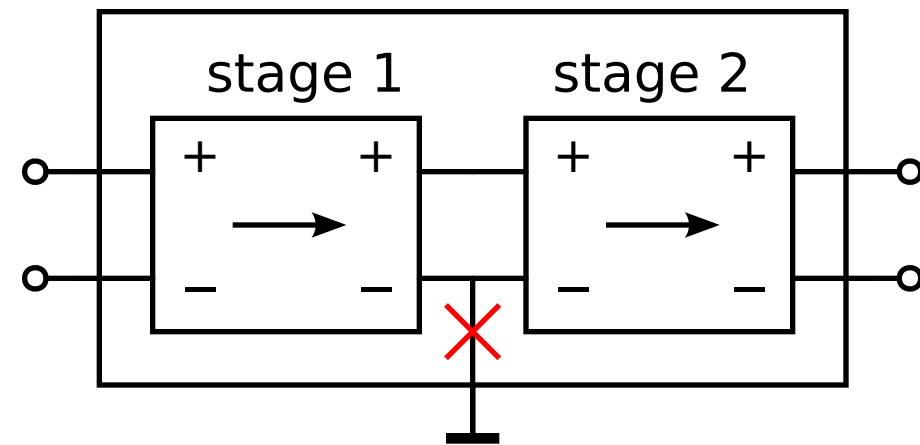
Two-port conditions no longer valid.

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Controller may not longer behave as a nullor for infinite loop gain

Interconnection of stages

Port isolation considerations

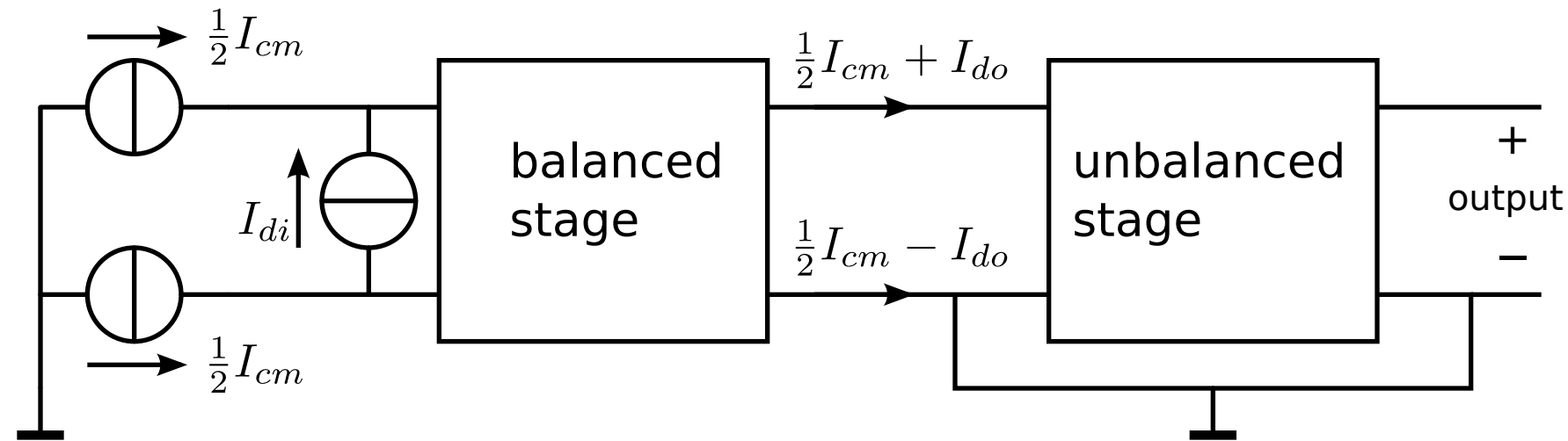


Internal ground connection:

Two-port conditions no longer valid.

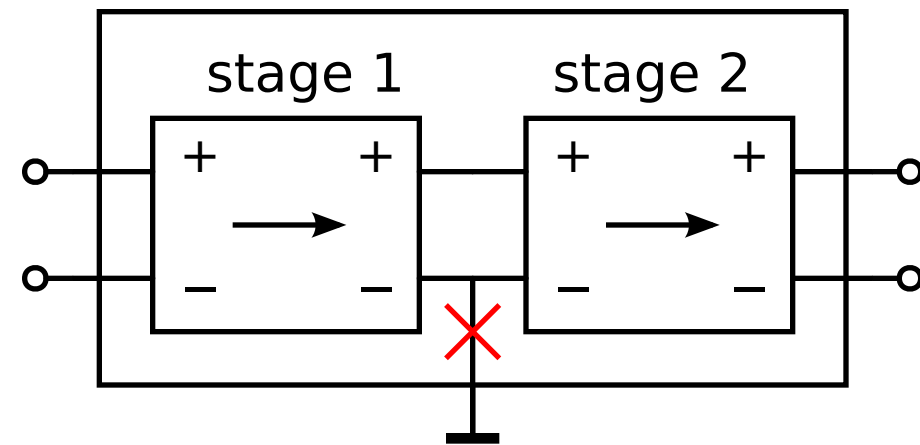
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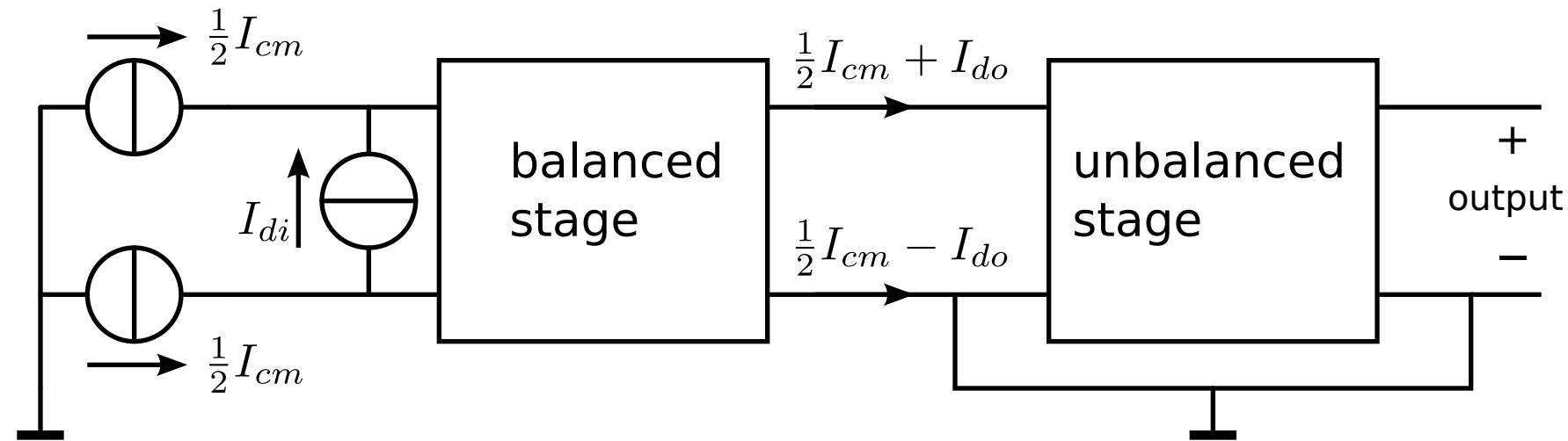


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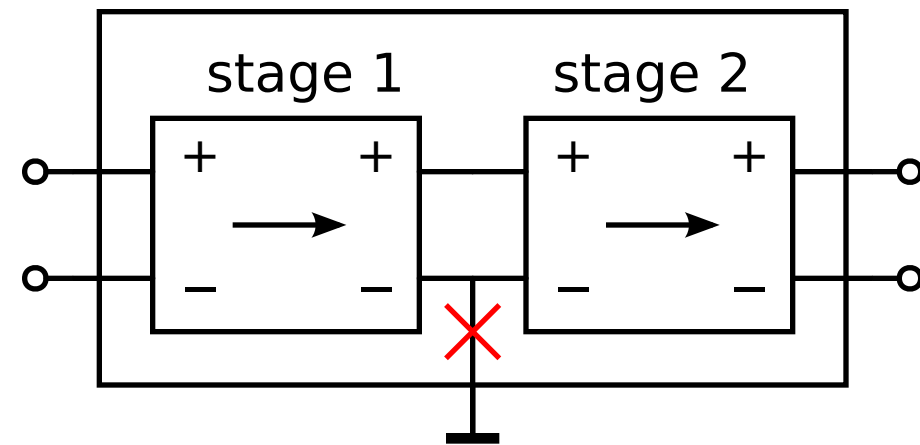
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Nonzero common-mode transfer:

Interconnection of stages

Port isolation considerations

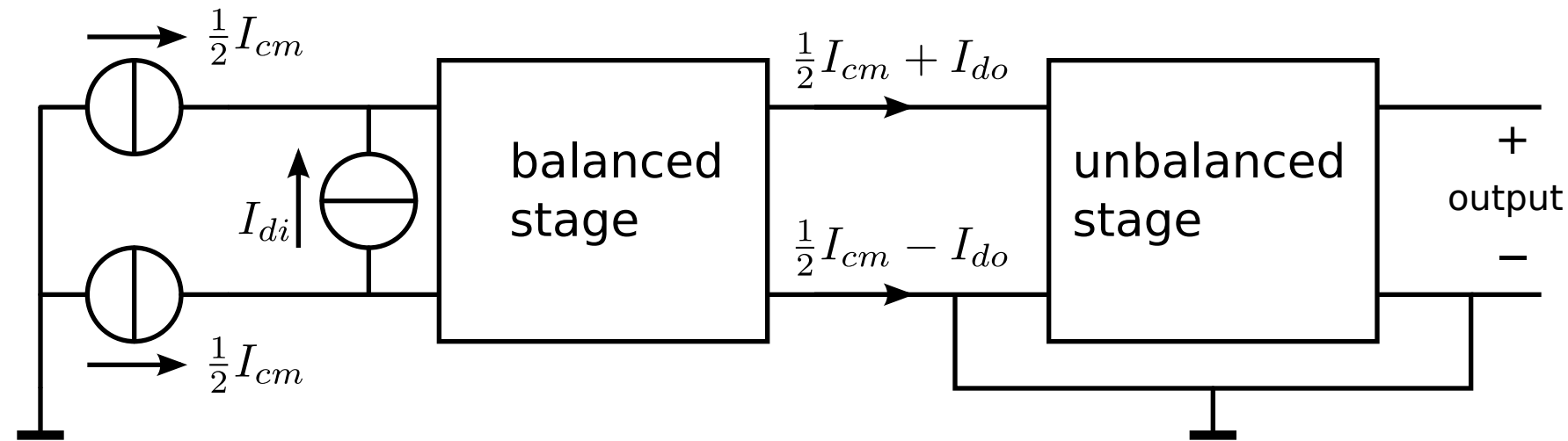


Internal ground connection:

Two-port conditions no longer valid.

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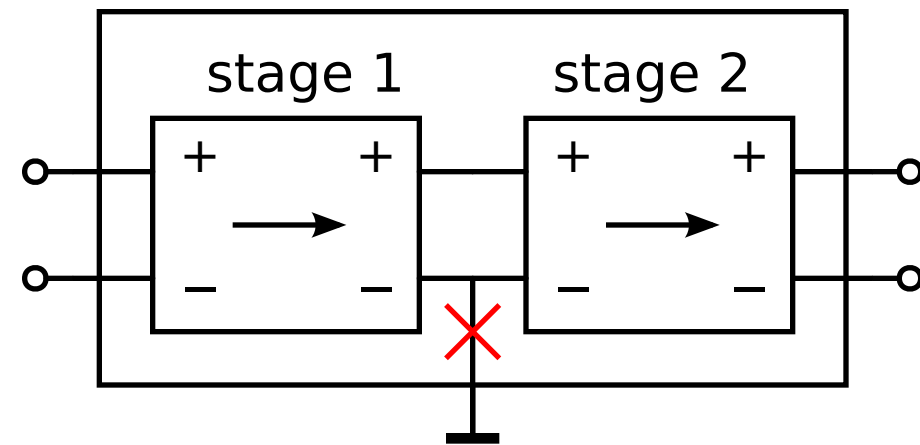


Nonzero common-mode transfer:

Possible limitation of the CMRR

Interconnection of stages

Port isolation considerations

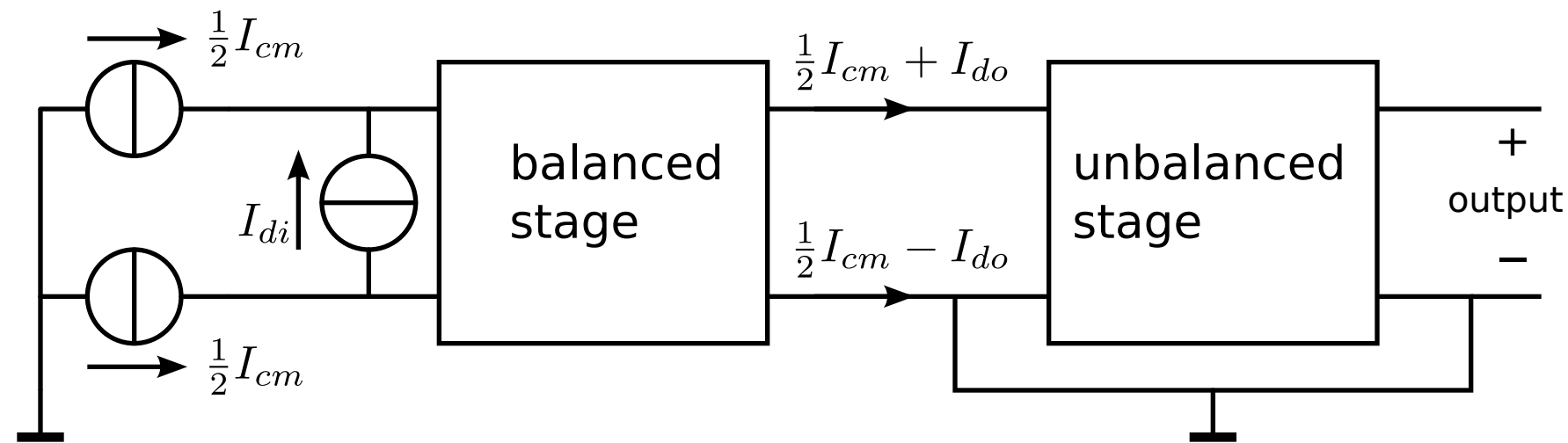


Internal ground connection:

Two-port conditions no longer valid.

Ideal gain may differ from asymptotic gain

Controller may not longer behave as a nullor for infinite loop gain



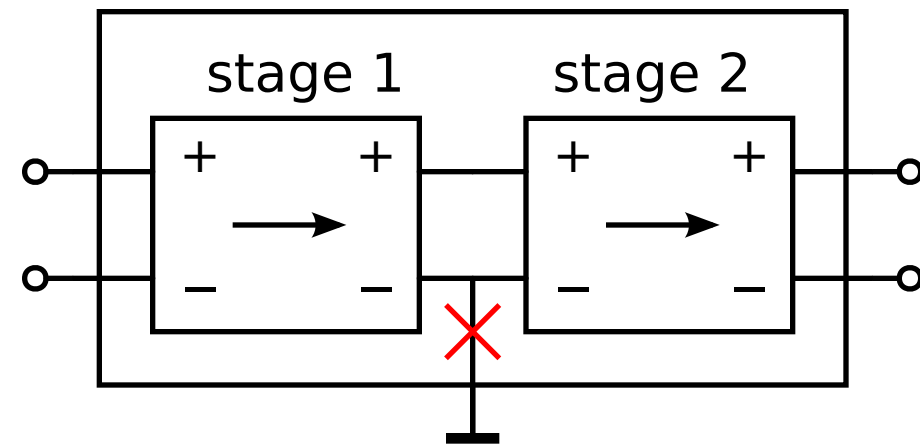
Nonzero common-mode transfer:

Possible limitation of the CMRR

If a common-mode signal is converted into a differential mode signal

Interconnection of stages

Port isolation considerations

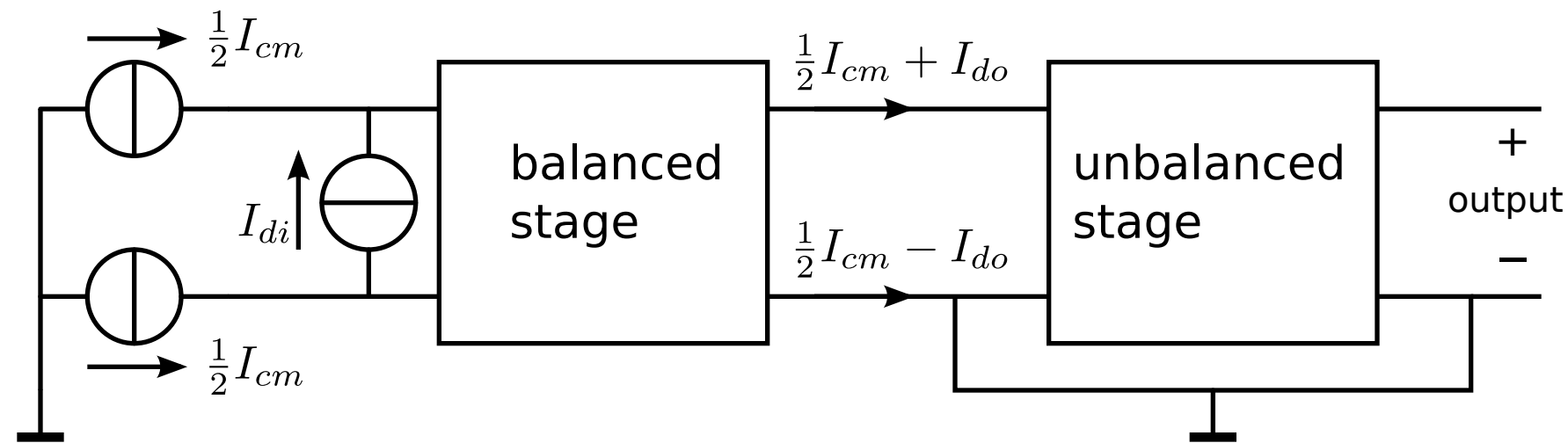


Internal ground connection:

Two-port conditions no longer valid.

Ideal gain may differ from asymptotic gain

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Nonzero common-mode transfer:

Possible limitation of the CMRR

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