Structured Electronic Design

Capacitively Loaded CC-stage

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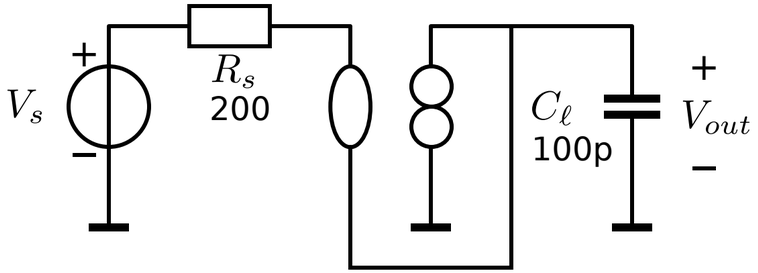
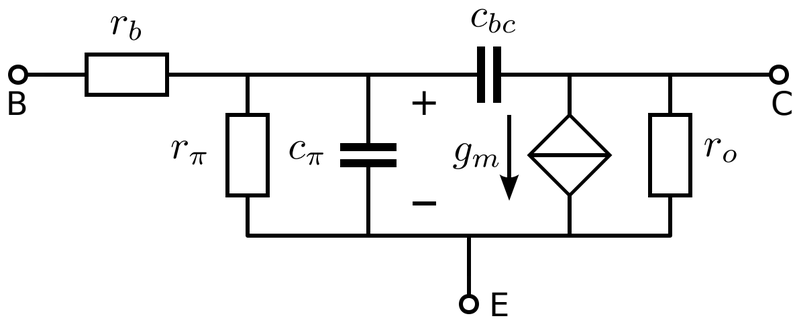
Capacitively loaded CC stage

Concept:
capacitively loaded voltage follower



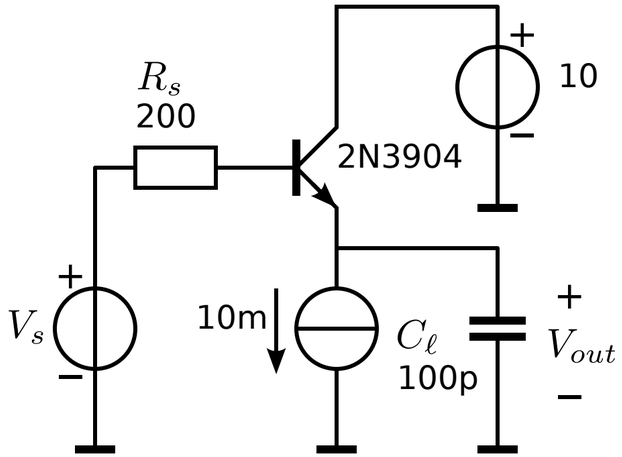
small-signal hybrid-pi equivalent circuit of a biased transistor



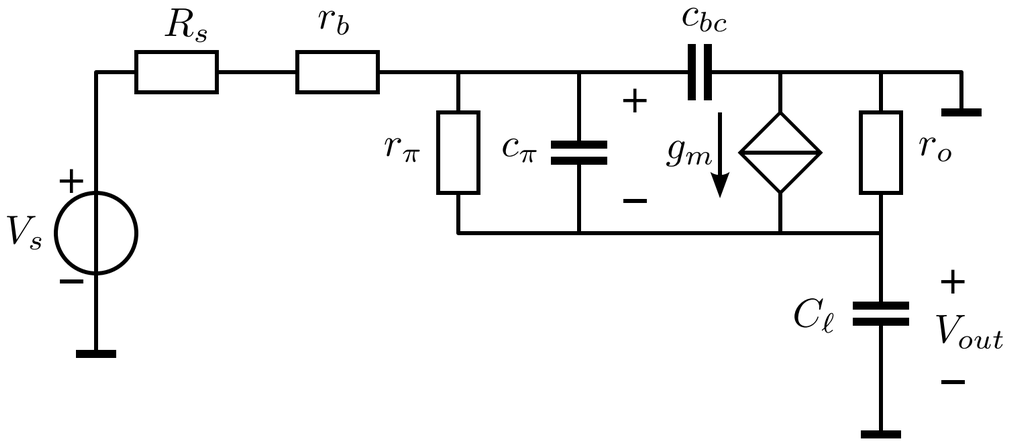
LTspice .op

Name:	q1
Model:	2n3904
Ib:	3.09e-05
Ic:	9.97e-03
Vbe:	7.14e-01
Vbc:	-1.00e+01
Vce:	1.07e+01
BetaDC:	3.23e+02
Gm:	3.77e-01
Rpi:	8.37e+02
Rx:	2.00e+01
Ro:	1.10e+04
Cbe:	1.45e-10
Cbc:	1.66e-12
Cjs:	0.00e+00
BetaAC:	3.16e+02
Cbx:	0.00e+00
Ft:	4.09e+08

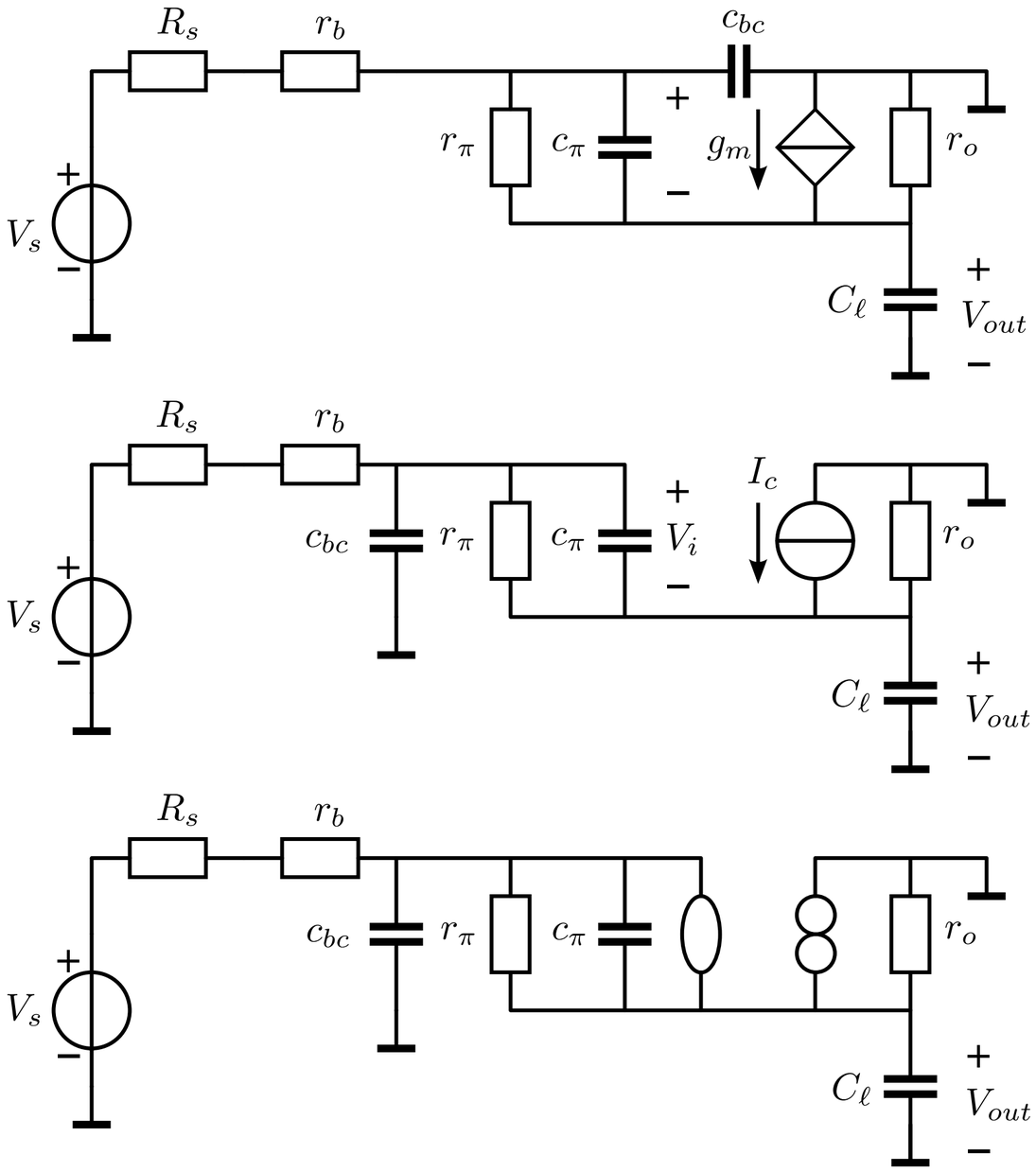
Implementation with BJT
Biased CE-stage is used as controller:



small-signal equivalent circuit of the capacitively loaded CC-stage



Asymptotic-gain model selection loop gain reference



Complete small-signal equivalent circuit

Controlled source selected as loopgain reference

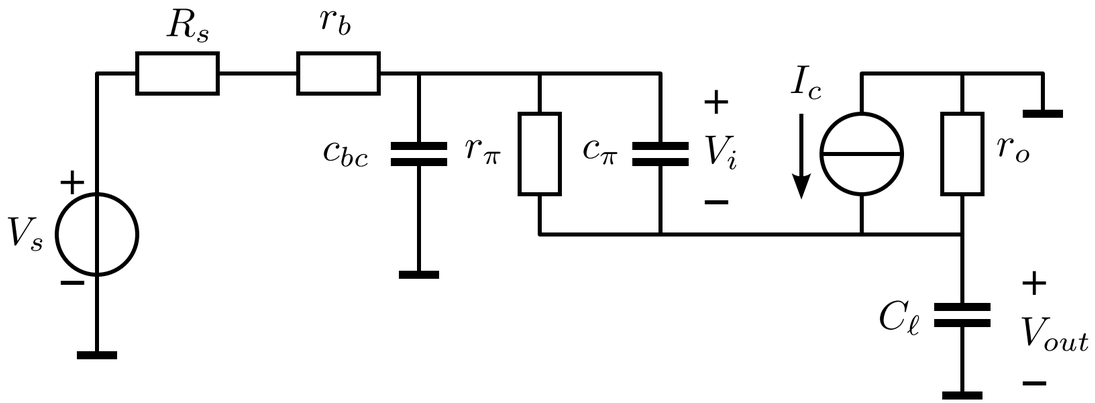
c_bc causes internal feedback loop

- can be placed outside the controller
- changes the ideal gain

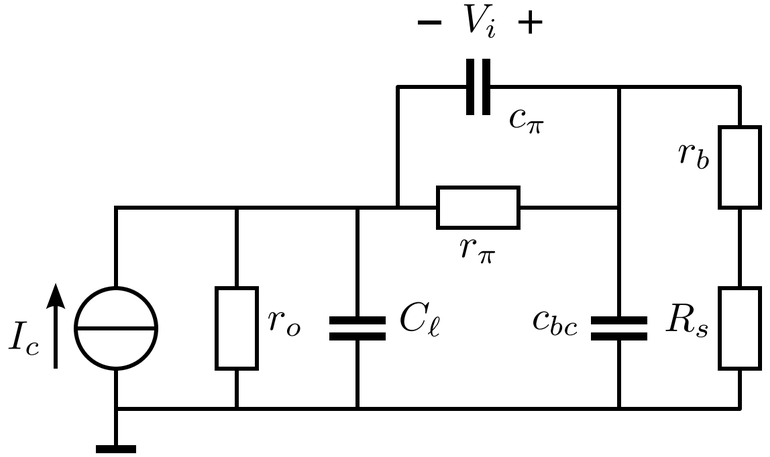
asymptotic-gain equals the ideal gain

$$\frac{V_{out}}{V_s} = \frac{1}{1+s(R_s+r_b)c_{bc}}$$

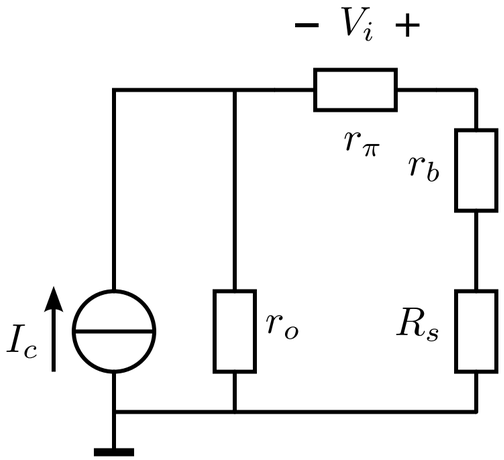
Evaluation DC loop gain



redraw the circuit



DC equivalent circuit



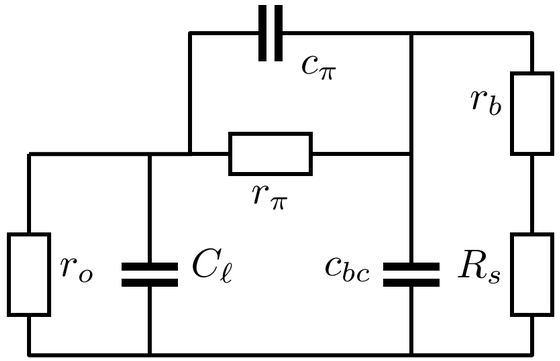
$$L_{DC} = -g_m \frac{r_o}{r_o+r_b+R_s+r_\pi} r_\pi = -\beta_{AC} \frac{r_o}{r_o+r_b+R_s+r_\pi}$$

$$L_{DC} = -288$$

current gain

current division

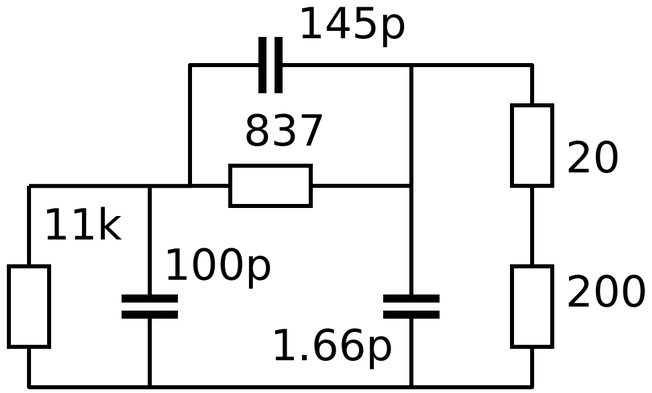
Evaluation poles loop gain



How many poles?

number of capacitors - number of independent loops of capacitors (and voltage sources)

two

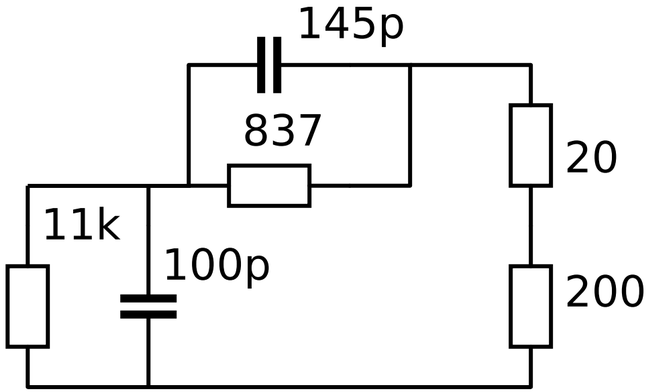


Method

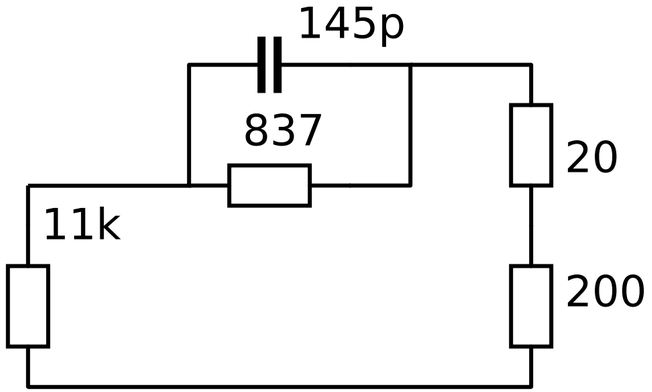
Leave c_{bc} out (much smaller than the equivalent series capacitance of the other two)

Use time-constant method for estimation of poles

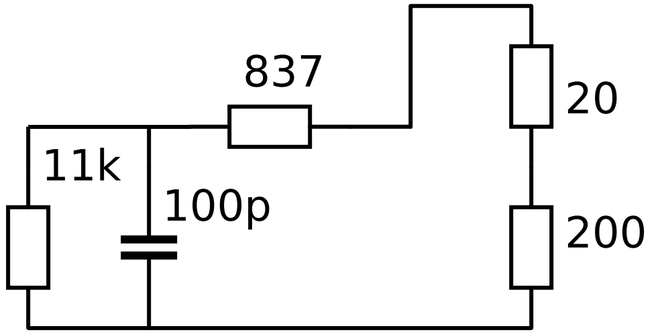
Evaluation poles loop gain



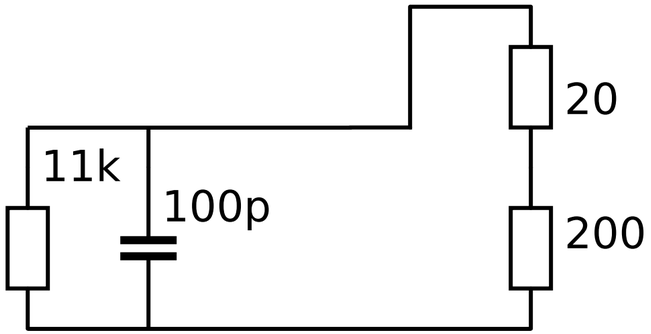
Leave c_{bc} out



Determine TC1:
145p // 837 // 11220 = 113ns



Determine TC2:
100p // 11000 // 1057 = 96ns



Short port with dominant time-constant and update TC2:
100p // 11000 // 220 = 21.6ns

$$p_1 = -\frac{10^9}{2\pi 113} = -1.41 \text{ MHz}$$

$$p_2 = -\frac{10^9}{2\pi 21.6} = -7.37 \text{ MHz}$$

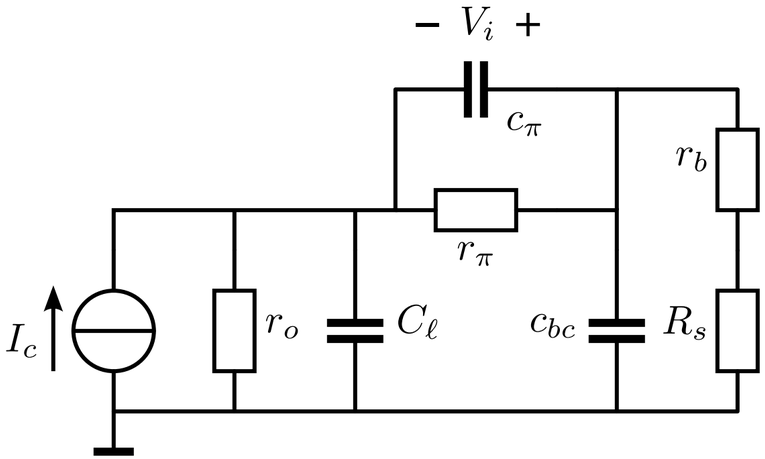
$$L_{DC} = -288$$

$$p_1 + p_2 = -8.78 \text{ MHz}$$

$$B_f = 54.8 \text{ MHz}$$

Sum of the poles much smaller than sqrt(2) times the bandwidth.
MFM response requires frequency compensation!

Evaluation zeros of loop gain



Zero at frequency where:

$$\frac{V_i}{I_c} = 0$$

if: $$\frac{1}{r_b + R_s} = -s\, c_{bc}$$

$$z = -\frac{1}{c_{bc}(R_s + r_b)}$$

Frequency of the zero: -436 MHz

Poles and zeros of loop gain, conclusions

Zero matches SLiCAP simulation

Product of the poles (bandwidth) matches SLiCAP simulation

Sum of the poles wrong (higher order approximation required)

Sum of the (dominant) poles not much of interest for design of bandwidth

Accurate analysis and phantom-zero compensation: see SLiCAP example