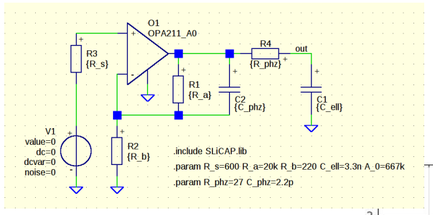
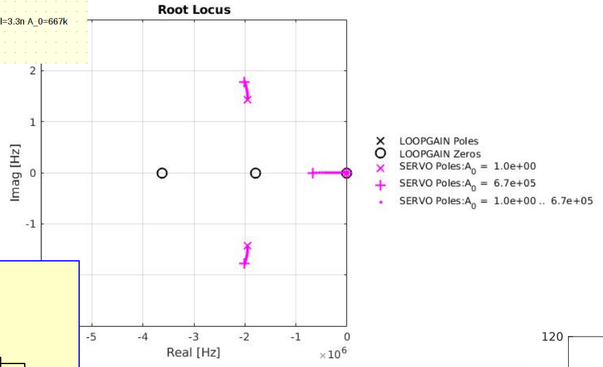
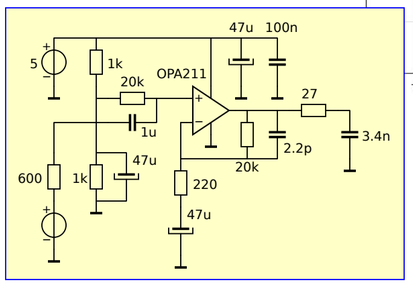
EE3C11: Structured Electronic Design
My First Voltage Amplifier
Design example EE3C11







SLiCAP project: myFirstVamp

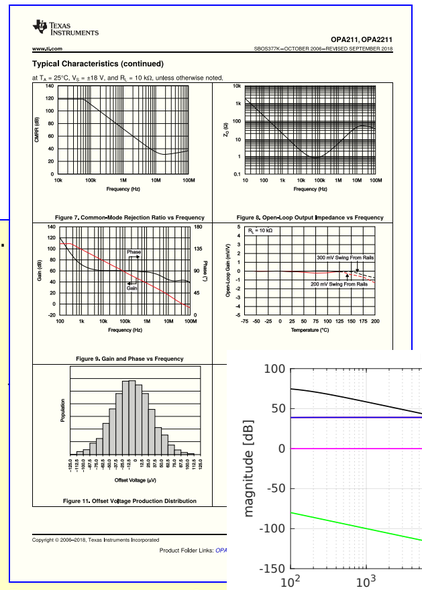
Table of contents

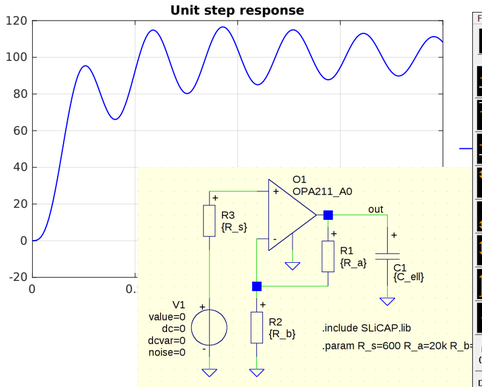
1. myFirstVampOPA211uncompensated
2. myFirstVampOPA211compensated
3. myFirstVampOPA211bias
4. myFirstVampOPA211complete
5. myFirstVampOPA211completeNoise

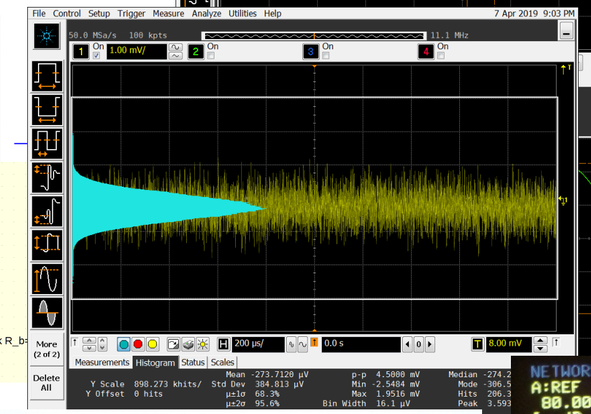
Go to main index

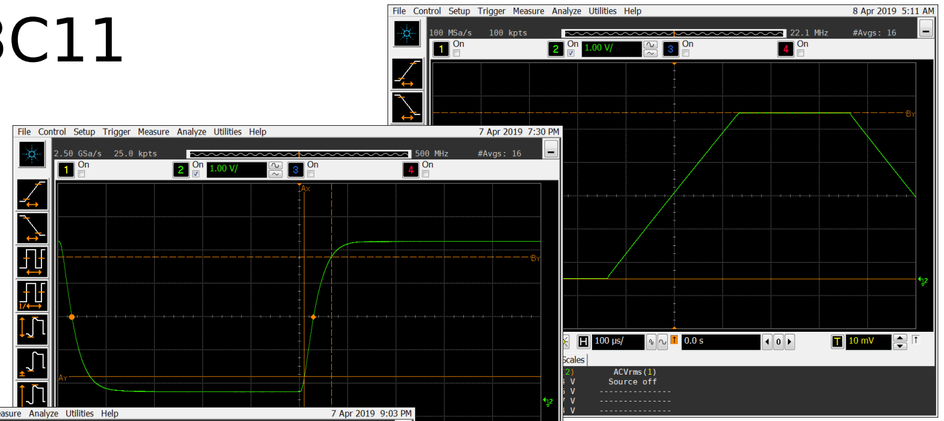
SLiCAP: Symbolic Linear Circuit Analysis Program, Version 0.6 © 2009-2019 Anton Montagne

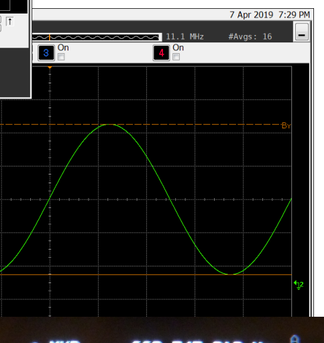
For documentation, examples, support, updates and courses please visit: analog-electronics.eu









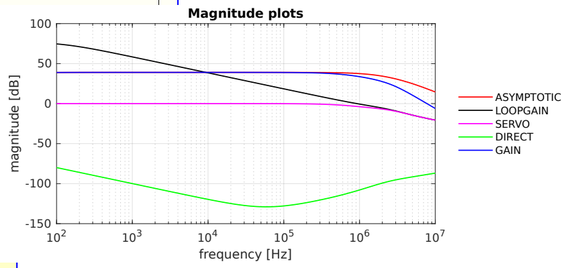



```
Checking circuit: myFirstVampCompensated.
No errors found!
    GAIN
    DC value = 9.189e+01
    Poles:
```

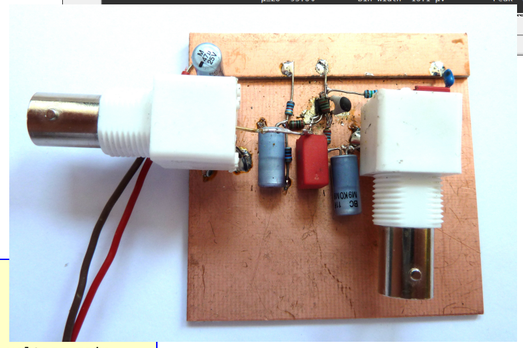
	RealPart	ImagPart
p_1	-7.8738e+05	0
p_2	-1.6015e+06	1.9166e+06
p_3	-1.6015e+06	-1.9166e+06
p_4	-1.9604e+07	0
p_5	-2.383e+07	0
p_6	-5.0504e+08	0

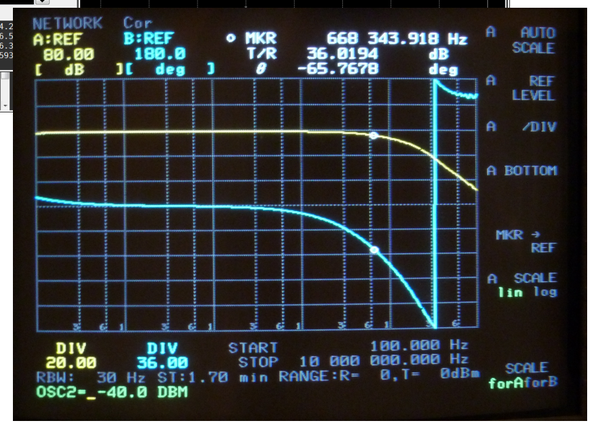
Zeros:

	RealPart	ImagPart	Frequency	Q
z_1	-1.061e+07	0	1.061e+07	0
z_2	-3.9963e+07	0	3.9963e+07	0
z_3	-8.0941e+08	-7.4266e+08	1.0985e+09	0.67858
z_4	-8.0941e+08	7.4266e+08	1.0985e+09	0.67858

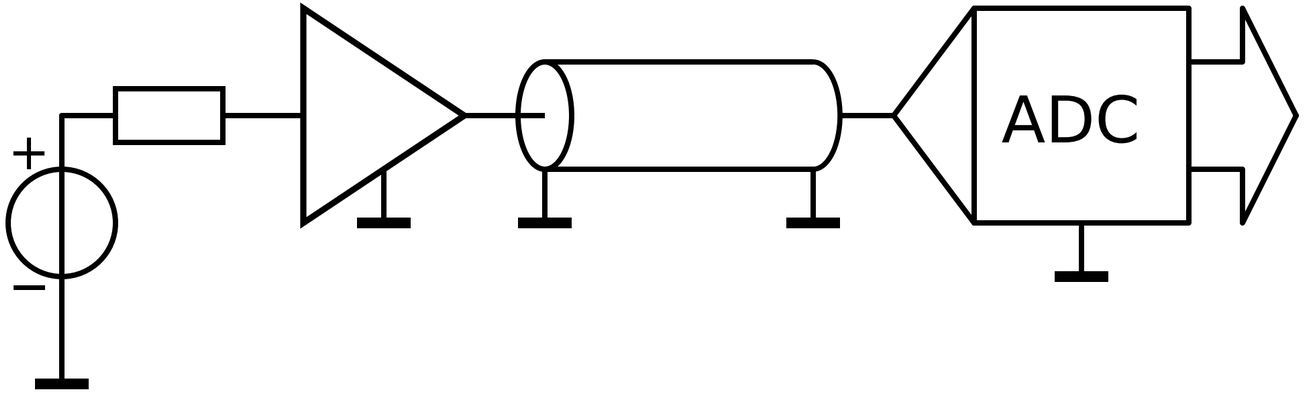



```
.model OPA211_A0 OV
+ cd = 8p  ; differential-mode input capacitance
+ gd = 50u ; differential-mode input conductance
+ cc = 2p  ; common-mode input capacitance
+ av = {A_0*(1+s/2/PI/40M)/(1+s/2/PI/120)/(1+s/2/PI/20M)}   ; voltage gain
+ zo = {3.6k/(1+s*3.6k*8u) + 0.7 + s*900n*60/(60+s*900n)}   ; output impedance
```





Application and initial specification



Signal source: voltage, mean value=0, max. deviation +/- 25mV_p

Source impedance: resistive, about 600 Ohm

Load: voltage mean value = 2.5V max. deviation +/- 2.25V_p

Load impedance: capacitive, up to 3.4nF

Small-signal bandwidth: 100Hz ... 500kHz

Full-power bandwidth: >= 100kHz

Noise figure < 3dB

Supply voltage: 5V

Operating temperature: room temperature

Engineering characteristics

Amplifier performance requirements

P1 Input impedance	>> 600 Ohm
P2 Input voltage	50 mV_{pp}
P3 Load capacitance	3400 pF
P4 Quiescent load voltage	2.5 V_{DC}
P5 Load signal voltage	4.5 V_{pp}
P6 Rate of change output voltage	>=1.41 V/us
P7 Noise figure @ 600 Ohm	<= 3 dB
P8 Small-signal bandwidth	100Hz ... 500kHz
P9 Gain and bias inaccuracy	<= 3%

Cost factors

C1 Power supply voltage	5 V_{DC}

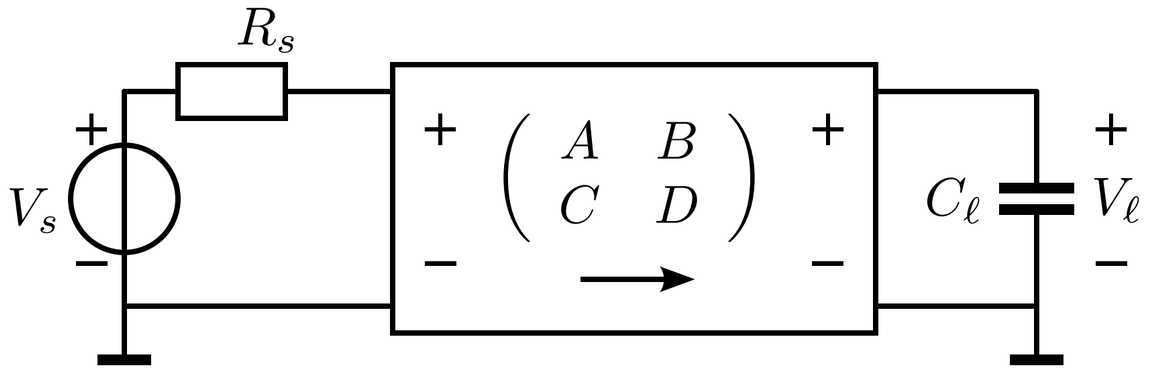
Environmental conditions

E1 Operating temperature	20 deg. Celsius

Design of amplifier configuration

Voltage transfer independent of source and load impedance.

$$A_v = \frac{V_\ell}{V_s} = \frac{4.5}{0.05} = 90$$



$$A = \frac{1}{A_v},\ B = 0,\ C = 0,\ D = 0$$

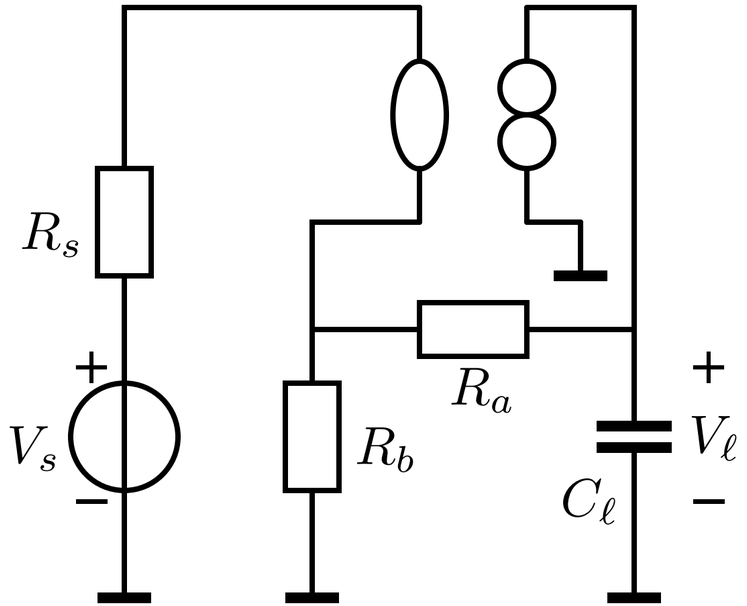
Amplifier concept for establishing a nonzero value for A only

Best performance with nonenergic feedback

- Wide-band transformer expensive

Passive feedback configuration

- Feedback network increases noise and power losses of controller



Nonzero value for A:

Parallel sensing

- Zero output impedance

Series comparison

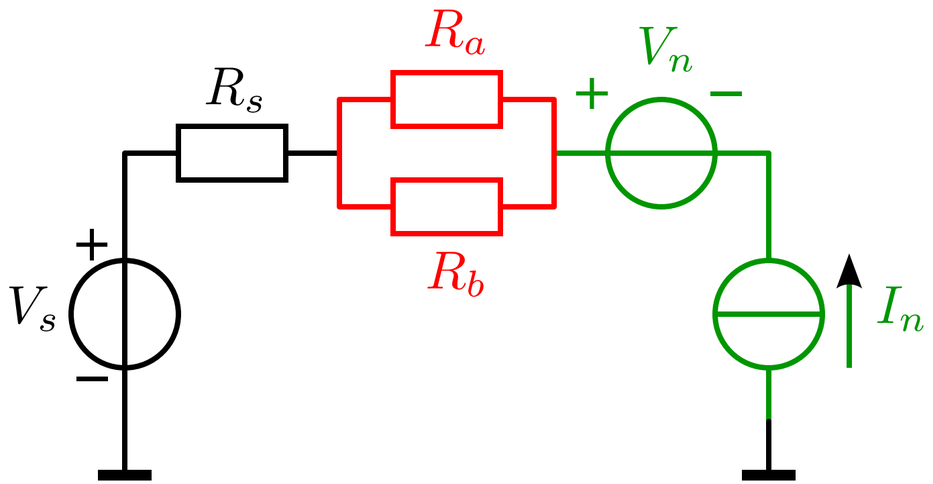
- Infinite input impedance

Noise design

Find and solve design equations for elements that contribute to the noise

1. Feedback resistors
2. Controller equivalent intput noise sources

Noise model:



$$S_{v_{tot}} = 4kT\left(R_s + R_a||R_b\right) + S_{V_n} + S_{I_n}\left(R_s + R_a||R_b\right)^2$$

Noise figure of 3dB:

$$S_{v_{tot}} = 8kTR_s$$

Show stopper values:

$R_a\|\|R_b < R_s$	600Ω
$S_{V_n} < 4kTR_s$	$3.15\frac{\text{nV}}{\sqrt{\text{Hz}}}$
$S_{I_n} < \frac{4kT}{R_s}$	$5.25\frac{\text{pA}}{\sqrt{\text{Hz}}}$

Voltage and current drive capability

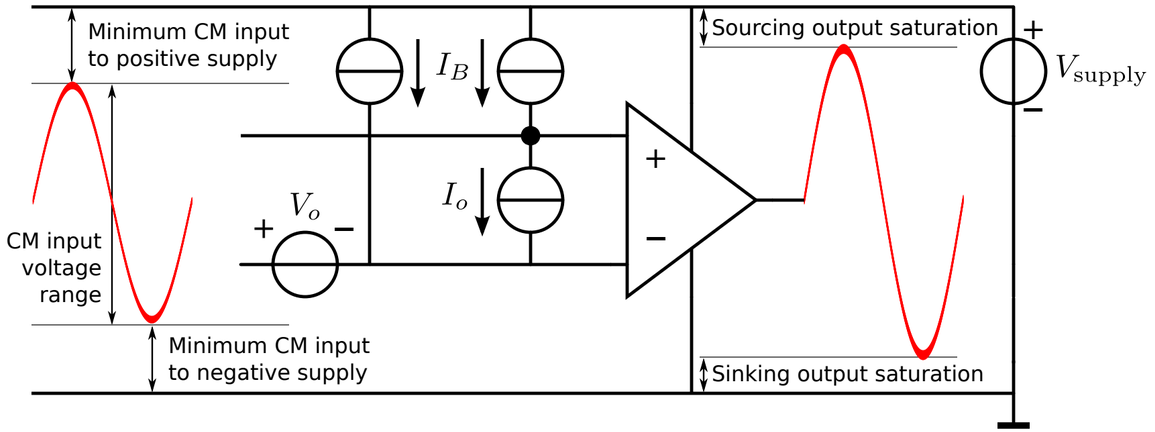
Voltage and current drive capability

Load drive requirements

Load signal voltage: $4.5V_{pp}$
Maximum rate of change @ 100kHz sine wave, $4.5V_{pp}$: 1.41 V/us
Maximum load current @ 100kHz sine wave, 4.5Vpp, 3.4nF: 4.8mA
Quiescent output voltage: 2.5V

Supply requirements

Supply voltage: 5V
No power consumption requirements



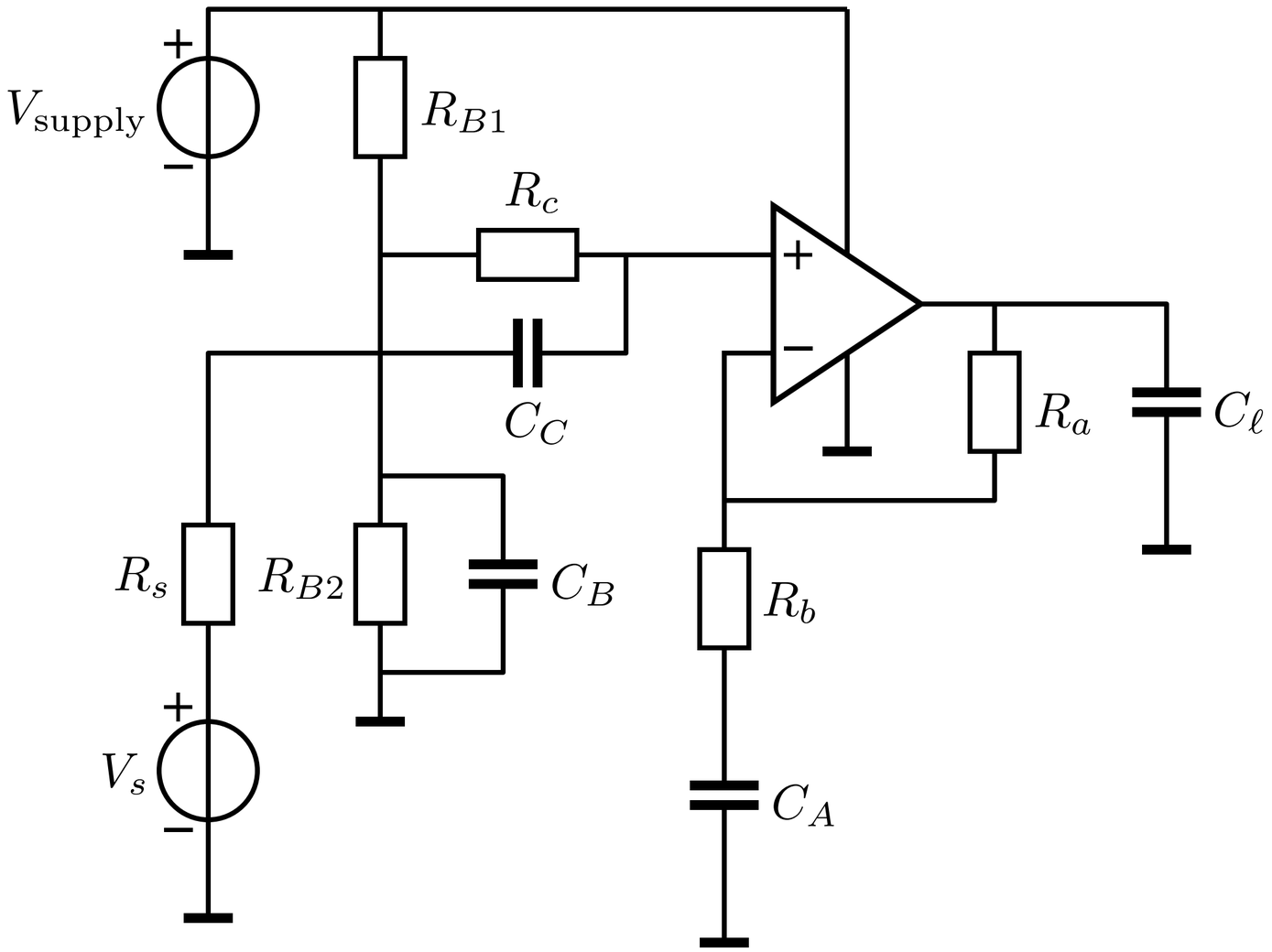
Biasing errors take a part of the budget for the total voltage drop

Biasing concept with AC coupling
As presented in Chapter 9

OpAmp requirements

Supply voltage: 5V
Current drive capability: > 4.8mA + current through feedback network
Output saturation source/sink: < 0.25V - total output biasing error voltage

Biasing errors



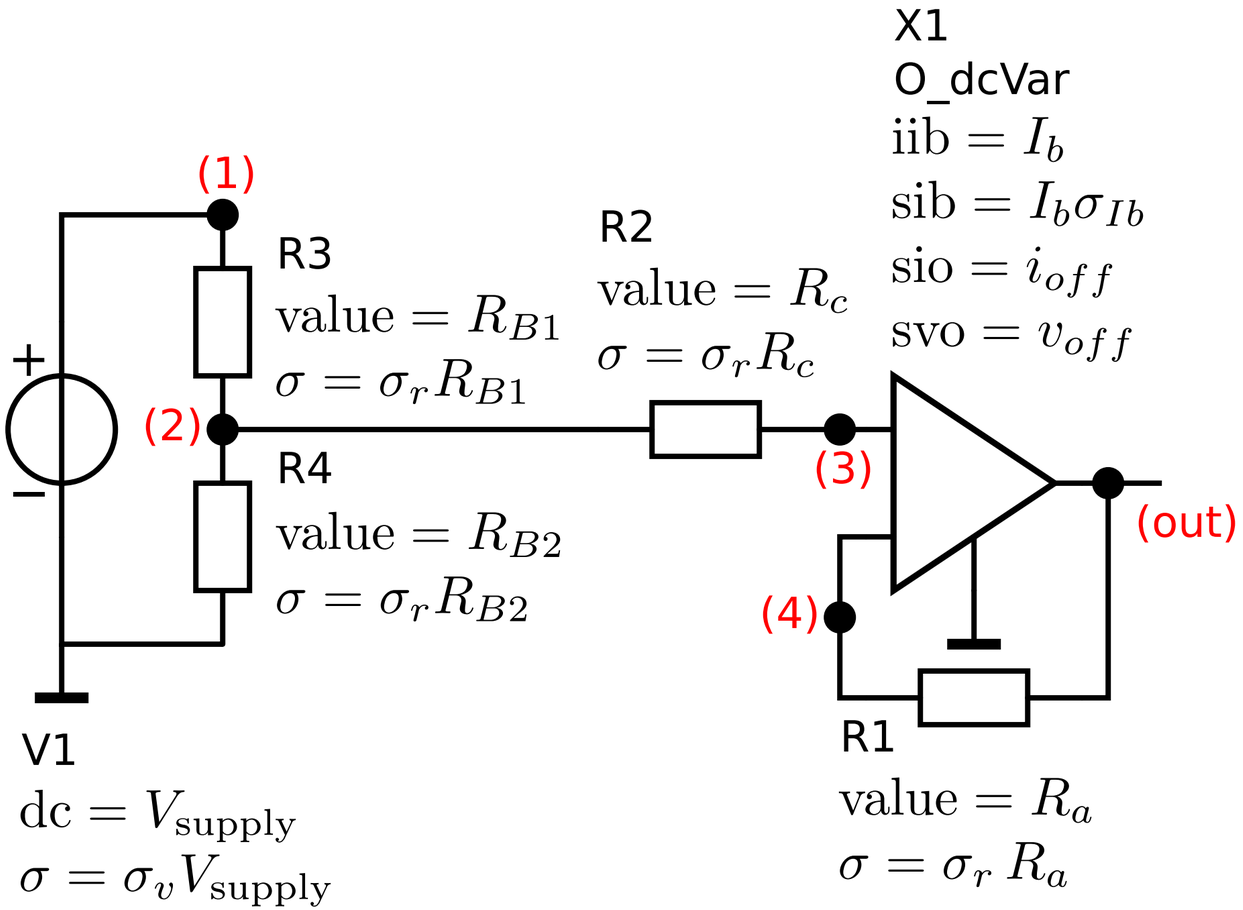
Contributions to biasing errors:

- Supply voltage tolerance
- Resistor tolerances
- Bias current OpAmp
- Offset current OpAmp
- Offset voltage OpAmp

Interaction with other performance aspects:

- Noise: $R_c \gg R_s,\ \frac{1}{2\pi f C_C} \ll R_s$
- Bandwidth: $\frac{1}{2\pi f_{\text{low}} C_A} \leq R_b$
- Accuracy: $R_c \gg R_s$
- PSRR: $\frac{1}{2\pi f_{\text{low}} C_B} \leq (R_b || R_a)$

Biasing errors



Simplified result: $R_c \gg \frac{R_{B1} R_{B2}}{R_{B1}+R_{B2}}$

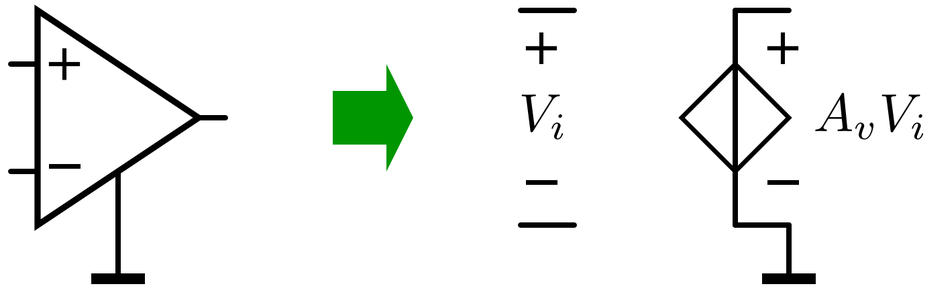
$$\sigma^2_{Vout} = 2\sigma_r^2 \left(\frac{V_s}{R_{B1}+R_{B2}}\right)^2 \left(\frac{R_{B1}R_{B2}}{R_{B1}+R_{B2}}\right)^2 + \sigma_v^2 V^2_{\text{supply}} \left(\frac{R_{B2}}{R_{B1}+R_{B2}}\right)^2 + v_{off}^2 + i_{off}^2 \left(R_c + R_a\right)^2 + \sigma_{Ib}^2 I_b^2 \left(R_c - R_a\right)^2 + \sigma_r^2 I_b^2 \left(R_c^2 + R_a^2\right)$$

Bandwidth design

Determination of the required GB product of the OpAmp

Use the simplest model that provides this information:

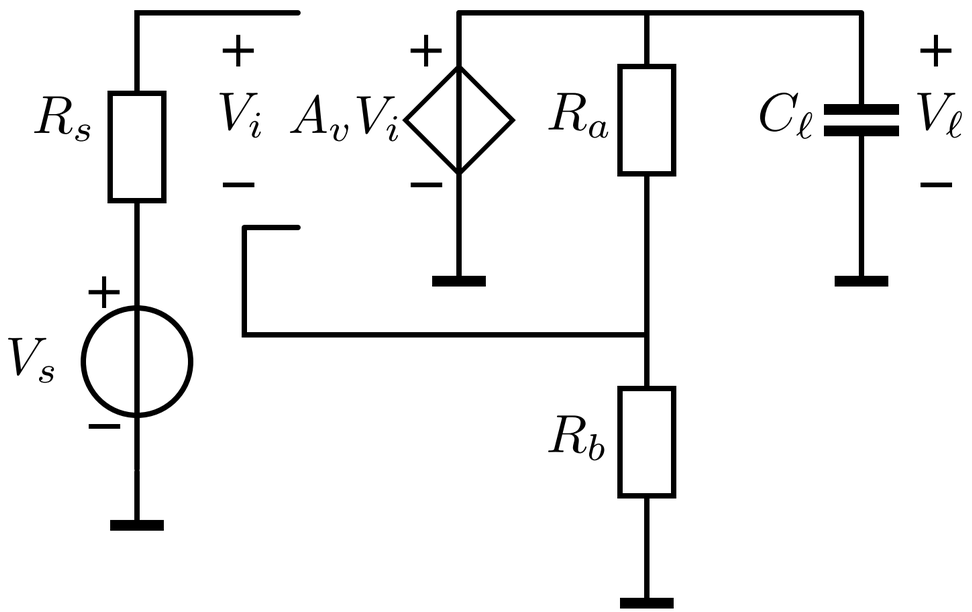
$$A_v = \frac{A_0}{1+s\frac{A_0}{2\pi \mathrm{GB}}}$$



Bandwidth design

Evaluation of loop gain-poles product

$$A_v = \frac{A_0}{1+s\frac{A_0}{2\pi \mathrm{GB}}}$$



$$L = -\frac{R_b}{R_a+R_b}\frac{A_0}{1+s\frac{A_0}{2\pi \mathrm{GB}}}$$

$$\mathrm{LP}_1 = \mathrm{GB}\frac{R_b}{R_a+R_b}[\mathrm{Hz}]$$

Achievable bandwidth B equals LP product:

$$\mathrm{GB} \geq \frac{R_a+R_b}{R_b}B[\mathrm{Hz}]$$

$$\mathrm{GB} \geq 45\ \mathrm{MHz}$$